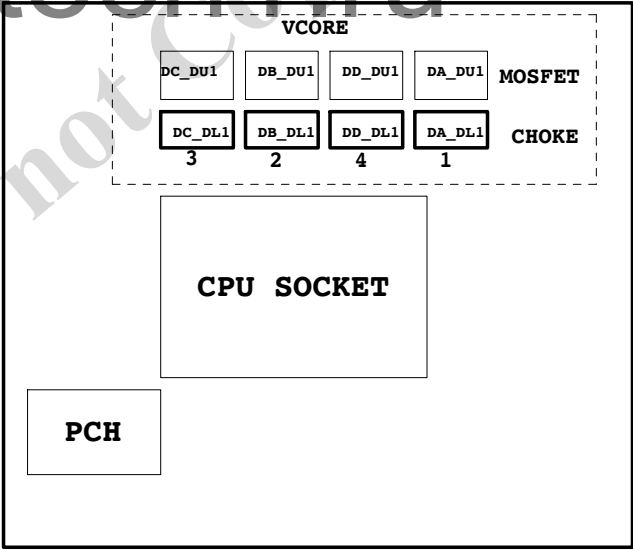


01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1150-A
05	CPU_LGA1150-B
06	CPU_LGA1150-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	PCH_FDI,DMI,USB,PCIE
10	PCH_RGB,CLK BUFFER
11	PCH_HOST,SATA,PCI
12	PCH_GPIO,CTRL,AUDIO
13	PCH_PWR,GND
14	PCI EXPRESS*16 SLOT
15	PCIEX1*2 , PCIEX4 SLOT
16	ITE8892 PCI BRIDGE
17	PCI SLOT 1&2
18	I/O ITE8728
19	COM, -PROHOT, R_USB
20	Dual BIOS , TPM SLB9635TT
21	ALC892 CODEC
22	REAR AUDIO JACK
23	VCORE PWM_IR3564a
24	VCORE+DDR PWM IR3553+IR3598
25	ME POWER
26	NCP3933 OVER VOLTAGE
27	DISCRETE POWER

28	F_PANEL , F_USB2.0/3.0
29	ATX POWER, CLOCK GEN
30	HWM , KB/MS , FAN CTRL
31	LAN INTEL i217
32	DVI
33	HDMI , R_USB30
34	TABLE LIST
35	
36	
37	
38	
39	
40	





## GA-H87-D3H

## Component value change history

Data	Change Item	Reason
0.1-0925	E-BOM	
	1. Z77-D3H改為削光黑PCB, slots同原本削光黑機種配色, CPU socket鍍黑	
	2. 8 series IR digital power PWM因Intel spec change, 須改用b版 (必須發行Firmware)	
	3. H77-D3H 注意上H87 chips,上ME power,咖啡黑機種配色,CPU socket standard,clock buffer要上	
	3. H77-D3H GPIO37 需Pull up to 3VDUAL	
0.2	1. Load-line DAR47 2.06K --> 2.37K , DAR46/50 1.4K --> 1.6K , DAC17 150P --> 100P	
	2. N_-LAN_WAKE NR60 8.2K/4 --> 1K/4/1	
	3. DA_DU1,DB_DU1,DD_DU1,DC_DU1 10IFB-403553-01R --> OTA1-603551-00R	
	4. DDR CHOKE阻值調整	
	5. CPU SOCKET + RM 要用新料號?	
0.2B	1. 確定Power stage用料:IR3553 or IR3550 or 3551?	
	2. GPIO8 "NR136"不上	
	3. Add +12V排阻 RN2-RN6	
0.2C	1. HU1 , HU2 level shifter change to NXP	
0.3	1. PWM MOSFET修改 IR3564B + power stage 改成 IR3564B + IR3535 + power pak (Cancel)	
	3. PWM MOSFET修改 IR3564B + power stage 改成 IR3564B + IR3535 + power pak	
1.0	1. PCIEX16 patch reset circuit 怎麼上?	
	2. Prochot是否只上一組	
	3. PCH_HS & MOS_HS change new 料號	
	4. 因DII 2222禁用, 注意Z87-D3H試產時用Panjit 2222是否可用 (BOM已內建)	
	5. HDMI/DVI change to NXP level shifter	
	6. CHECK 5VSB保護線路是否上件	
10A	1. PCB REV1.0 --> REV1.01	
	2. Update LAN: i217V料號	
	3. Add DAQ6,DAR81	
10B	1. Add M3 POWER For Remote wake on LAN	
10C	1. MOS_HS 12SP2-S08824-21R/22R/23R --> 12SP2-S08824-51R/52R/53R	
	2. Add PCB : 全成信	
11A	1. For H87 Rev.C2	
11B	1. Disable Anti-surge Function	
11C	1. 5VSB --> 5VDUAL OVP & Remove CD1:A22225	

## Circuit or PCB layout change

DATE	Change Item	Reason
0.1	E-BOM	
0.2	1. U8 pin3加粗40mils 2. Update LAYOUT NEW RULE for四層板 3. MDA6線長T型要統等長 4. N_GPIO37 pull up VCC3 --> 3VDUAL 5. CPU Thertrip CPU_VTT --> VCC1_05_PCH 6. 確認 R/G/B ESD擺放位置 7. Add PCIEX16 reset patch circuit 8. PCIE signal by group 成對走 9. VIN0 --> VCORE0 , VINS --> VCORE 10. CS 1pin --> 2pin 11. 後窗部份鋪銅會挖 + 字處理 12. Add MA_DR8 , MA_DC8單獨下地 13. add VTT_PWRGD control circit 14. Update F_PANEL footprint "H2X10PANEL-3" 15. NR132跟NC59 layout位置交換 16. Add DS_ME GP67 control 17. Q6位置靠近 PWM power control pin 18. WR59 change to "R0204-2" 19. 文字面 "DualBIOS" , 改為 "Dual UEFI BIOS" , Add "Intel GbE LAN" 20. MAU2 REF "GND" 21. DDR Choke ML1,ML2 1.2uH/20A --> 0.8uH/35A	
0.21	1. AUDIO SPDIF-IN CR77 "0402-2" FOR short protection 2. add AUDIO ON/OFF PLAYER 3. Change PCIEX1/PCIX4 CLK 4. Update F_PANEL footprint 5. CPU VRIN OV IO_GP81 --> IO_GP21	
0.3	1. PWM MOSFET修改 IR3564B + power stage 改成 IR3564B + IR3535 + power pak (Cancel)	
1.0	1. 0 ohm --> short pad 2. 簡化CPU Config setting 3. 預留N_PCH_DPWROK 控制線路 4. 注意Slot和後窗正面有做十字Thermal處理 5. NBC65移靠近PCH 6. Add R700-R702 for FAN short protection 7. PWR_LED 改為IO_GP65 8. VTT_PWRGD Update 9. N_GPIO37 pull-up to VCC3 10. +12V RN2-RN6 & VCC/VCC3/5VSB dummy load 排阻 11. DDR_15V H/W monitor detect 改從 DDR slot 拉回 12. 5VSB AD1要過 NET 13. DDR VIN 間隔拉開 , 背板GATE往上移 14. Add DDR_15V dummy load 15. 5VSB/5VDUAL OVP protection	
1.01	1. 0 ohm --> short pad 2. Remove "BIOS_PH" & "M_BIOS socket" & "CS" pin 3. Add MADQ6 4. USB3 port3/4 , 5/6 swap	

1.02

1. CPU FAN ADD 100uF  
2. DART2改成R0402-2(靠近DD DU1) ,DART4改成R0603-RH(放在DART2左邊) , RS1改成R0402-2  
3. Add DAR82 For MOSFET "PHSFLT-" protect

1.1

1. 改文字面Rev1.1 For Z87 Rev.C2  
2. 文字面UEFI DUALBIOS

1.2

1. ALL FAN ADD 0.1u/4  
2. PCH X TAL 25MHZ REF "GND"  
2. Add MF1 FUSE for VDDSPD

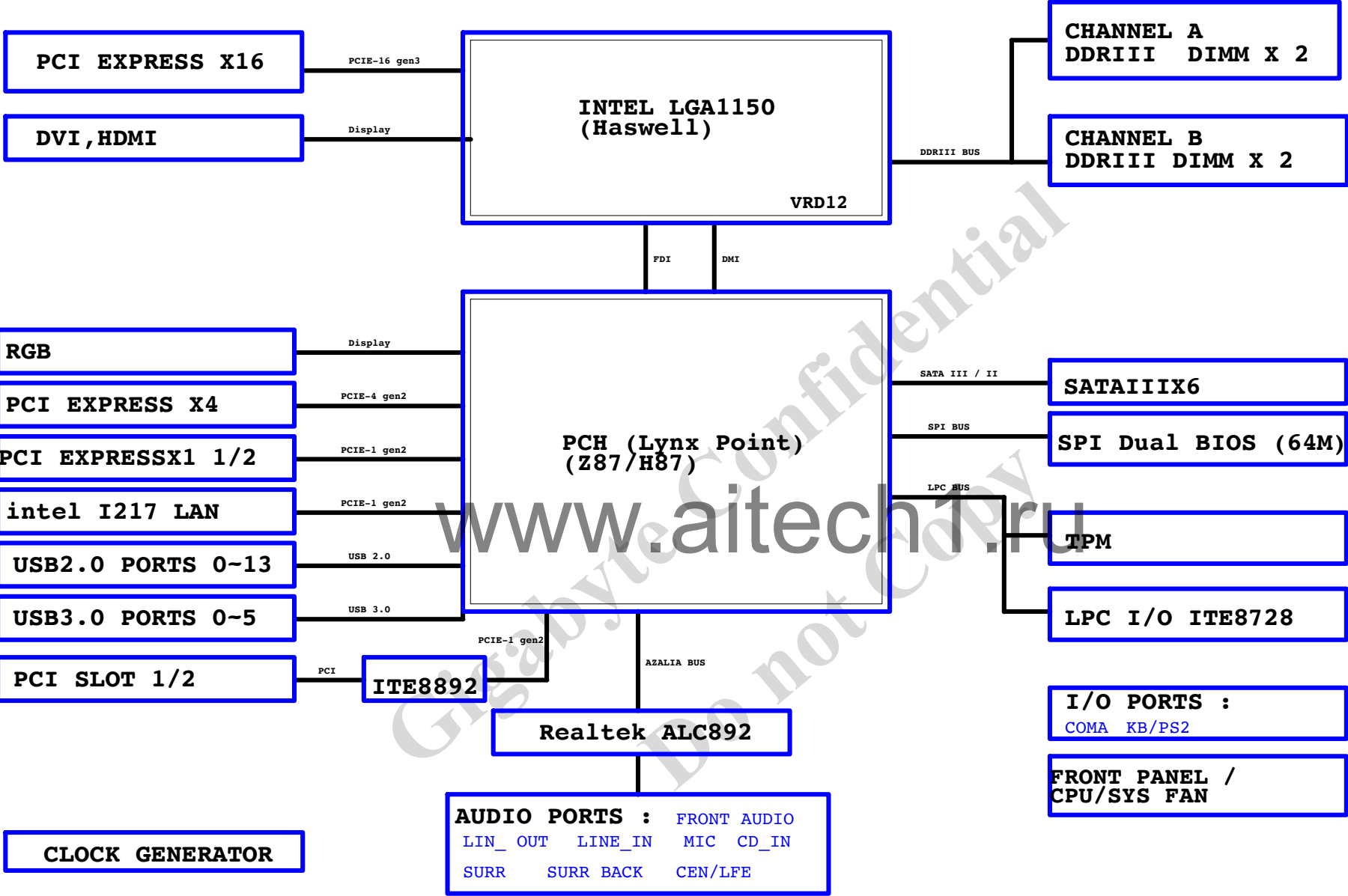
Gigabyte Technology

BOM &amp; PCB MODIFY HISTORY

Title	Document Number		Rev
Size	GA-H87-D3H		1.1
Date:	Tuesday, August 06, 2013	Sheet	2 of 34

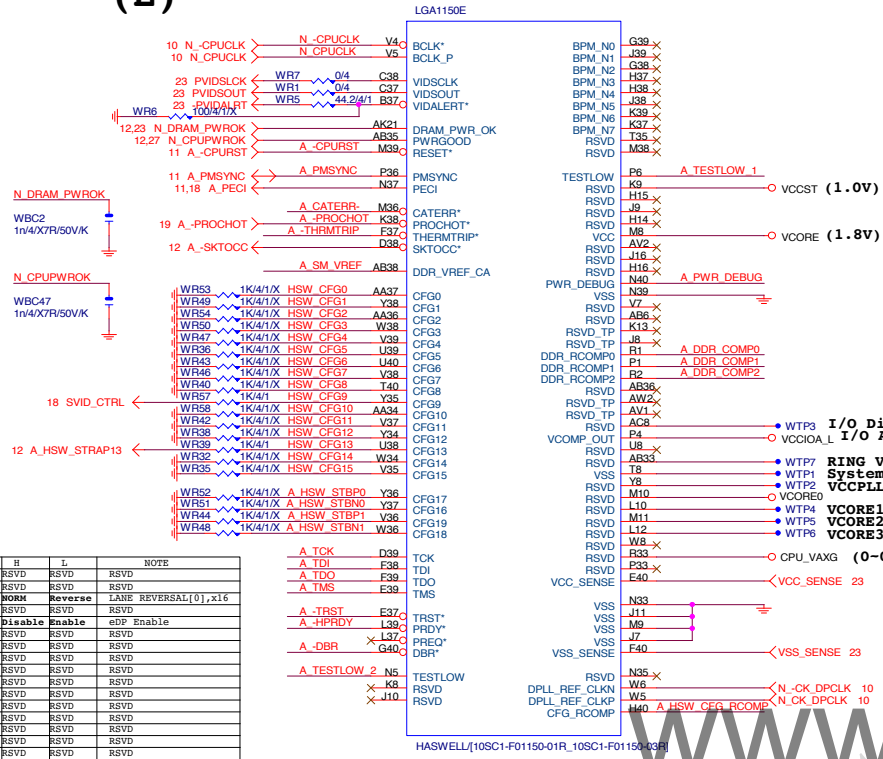


BLOCK DIAGRAM





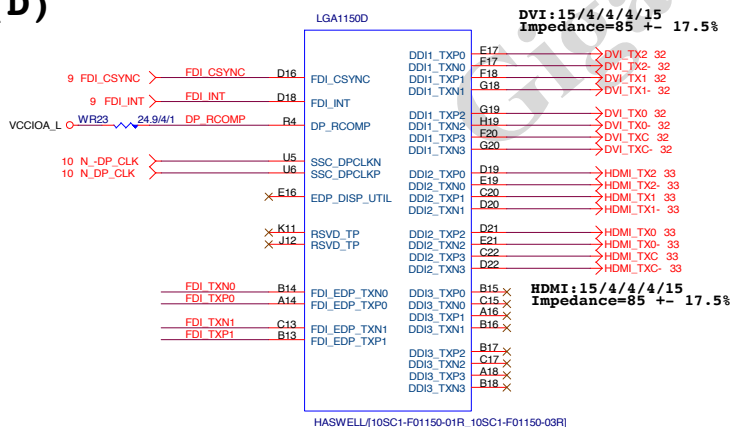
**LGA1150 (E)**



CFG	H	L	NOTE
0	RSVD	RSVD	RSVD
1	RSVD	RSVD	RSVD
2	<b>MORH</b>	<b>Reverse</b>	LANE REVERSAL[0],x16
3	RSVD	RSVD	RSVD
4	<b>Disable</b>	<b>Enable</b>	cDP Enable
7	RSVD	RSVD	RSVD
8	RSVD	RSVD	RSVD
9	RSVD	RSVD	RSVD
10	RSVD	RSVD	RSVD
11	RSVD	RSVD	RSVD
12	RSVD	RSVD	RSVD
13	RSVD	RSVD	RSVD
14	RSVD	RSVD	RSVD
15	RSVD	RSVD	RSVD
16	RSVD	RSVD	RSVD
17	RSVD	RSVD	RSVD

CFG 0-17 all internal PULL-UP

**LGA1150 (D)**



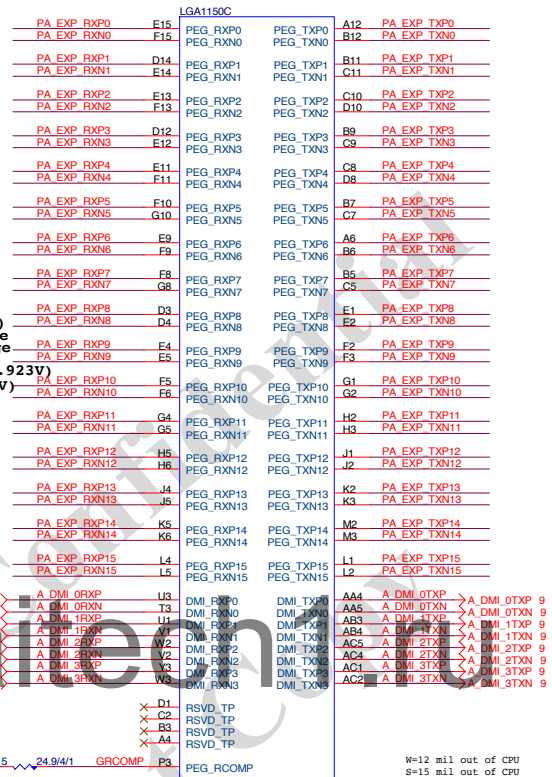
FDI:12/4/4/4/12 (breakout min 6/4/4/4/6)  
Impedance=85 +- 17.5%

FDI\_TXP[0..1] >> FDI\_TXP[0..1] 9

FDI\_TXN[0..1] >> FDI\_TXN[0..1] 9

**LGA1155** (C)

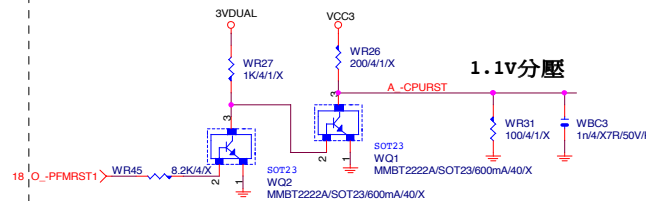
PCIEX16:20/5/4/5/20(breakout min 10/4/4/4/10)  
Impedance=80 +- 17.5%



DMI:12/4/4/4/12(breakout min 8/4/4/4/8)  
Impedance=85 +- 17.5%

PA EXP TXP[0..15]	>>	PA_EXP_TXP[0..15]	14
PA EXP TXN[0..15]	>>	PA_EXP_TXN[0..15]	14
PA EXP RXP[0..15]	>>	PA_EXP_RXP[0..15]	14
PA EXP RXN[0..15]	>>	PA_EXP_RXN[0..15]	14

**-CPURST**



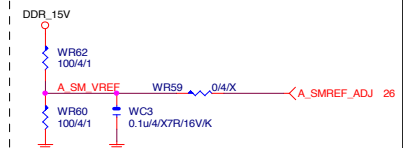
## CPU SVID



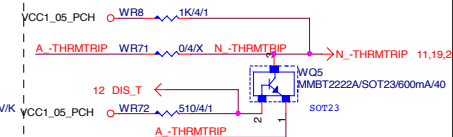
## CPU PU/PD



SM	REF
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**THRMTRIP DISABLE**



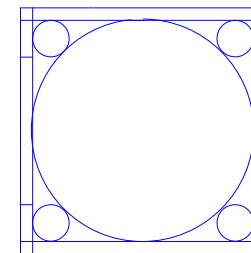


LGA1150A		DDR0_MA0	DDR0_D00	AD38	MDA0
MAAA0	AU13	DDR0_MA1	DDR0_D01	AD39	MDA1
MAAA1	AV16	DDR0_MA2	DDR0_D02	AF38	MDA2
MAAA2	AU16	DDR0_MA3	DDR0_D03	AF39	MDA3
MAAA3	AW17	DDR0_MA4	DDR0_D04	AD37	MDA4
MAAA4	AU17	DDR0_MA5	DDR0_D05	AD40	MDA5
MAAA5	AW18	DDR0_MA6	DDR0_D06	AE37	MDA6
MAAA6	AV17	DDR0_MA7	DDR0_D07	AF40	MDA7
MAAA7	AT18	DDR0_MA8	DDR0_D08	AH40	MDA9
MAAA8	AU18	DDR0_MA9	DDR0_D09	AH39	MDA10
MAAA9	AT19	DDR0_MA10	DDR0_D10	AK38	MDA10
MAAA10	AW11	DDR0_MA11	DDR0_D11	AK39	MDA11
MAAA11	AV19	DDR0_MA12	DDR0_D12	AH37	MDA12
MAAA12	AU19	DDR0_MA13	DDR0_D13	AH38	MDA12
MAAA13	AT20	DDR0_MA14	DDR0_D14	AK37	MDA14
MAAA14	AW21	DDR0_MA15	DDR0_D15	AK40	MDA15
MAAA15	AU21	DDR0_MA16	DDR0_D16	AM40	MDA17
MODT_A0	AW10	DDR0_ODT0	DDR0_D17	AM39	MDA21
MODT_A1	AV8	DDR0_ODT1	DDR0_D18	AP38	MDA18
MODT_A2	AW9	DDR0_ODT2	DDR0_D19	AP39	MDA19
MODT_A3	AU8	DDR0_ODT3	DDR0_D20	AM37	MDA20
			DDR0_D21	AM38	MDA16
			DDR0_D22	AP37	MDA22
			DDR0_D23	AP40	MDA23
			DDR0_D24	AV37	MDA25
			DDR0_D25	AW37	MDA28
			DDR0_D26	AU35	MDA26
			DDR0_D27	AT37	MDA27
			DDR0_D28	AT37	MDA28
			DDR0_D29	AT35	MDA30
			DDR0_D30	AW35	MDA31
			DDR0_D31	AY6	MDA33
			DDR0_D32	AU6	MDA37
			DDR0_D33	AV4	MDA34
			DDR0_D34	AU4	MDA35
			DDR0_D35	AW6	MDA36
			DDR0_D36	AW4	MDA38
			DDR0_D37	AR1	MDA39
			DDR0_D38	AR4	MDA45
			DDR0_D39	AN3	MDA42
			DDR0_D40	AN4	MDA43
			DDR0_D41	AR2	MDA44
			DDR0_D42	AR3	MDA40
			DDR0_D43	AN2	MDA46
			DDR0_D44	AN1	MDA47
			DDR0_D45	AL1	MDA49
			DDR0_D46	AL4	MDA53
			DDR0_D47	AL4	MDA50
			DDR0_D48	AJ4	MDA51
			DDR0_D49	AL2	MDA52
			DDR0_D50	AJ2	MDA48
			DDR0_D51	AJ2	MDA54
			DDR0_D52	AJ1	MDA55
			DDR0_D53	AG1	MDA57
			DDR0_D54	AG4	MDA61
			DDR0_D55	AE3	MDA58
			DDR0_D56	AE4	MDA59
			DDR0_D57	AG2	MDA60
			DDR0_D58	AG3	MDA56
			DDR0_D59	AE2	MDA63
			DDR0_D60	AE1	MDA62
			DDR0_D61	AE39	DQSA0
			DDR0_D62	AJ39	DQSA1
			DDR0_D63	AN39	DQSA2
			DDR0_D64	AV36	DQSA3
			DDR0_D65	AV5	DQSA4
			DDR0_D66	AP3	DQSA5
			DDR0_D67	AK3	DQSA6
			DDR0_D68	AF3	DQSA7
			DDR0_D69	AV32	DQSA0
			DDR0_D70	AE38	DQSA1
			DDR0_D71	AJ38	DQSA2
			DDR0_D72	AN38	DQSA3
			DDR0_D73	AJ36	DQSA4
			DDR0_D74	AW5	DQSA5
			DDR0_D75	AP2	DQSA6
			DDR0_D76	AK2	DQSA7
			DDR0_D77	AF2	DQSA7
			DDR0_D78	AU32	

HASWELL[10SC1-F01150-01R\_10SC1-F01150-03R]

LGA1150B		DDR1_MA0	DDR1_D00	AE34	MDB0
MAAB0	AL19	DDR1_MA1	DDR1_D01	AE35	MDB1
MAAB1	AK23	DDR1_MA2	DDR1_D02	AG35	MDB2
MAAB2	AM22	DDR1_MA3	DDR1_D03	AH35	MDB3
MAAB3	AM23	DDR1_MA4	DDR1_D04	AD34	MDB4
MAAB4	AP23	DDR1_MA5	DDR1_D05	AD35	MDB5
MAAB5	AL23	DDR1_MA6	DDR1_D06	AG34	MDB6
MAAB6	AY24	DDR1_MA7	DDR1_D07	AH34	MDB7
MAAB7	AV25	DDR1_MA8	DDR1_D08	AL34	MDB8
MAAB8	AU26	DDR1_MA9	DDR1_D09	AL35	MDB9
MAAB9	AW25	DDR1_MA10	DDR1_D10	AK31	MDB10
MAAB10	AP18	DDR1_MA11	DDR1_D11	AL31	MDB11
MAAB11	AY25	DDR1_MA12	DDR1_D12	AK34	MDB12
MAAB12	AV26	DDR1_MA13	DDR1_D13	AK35	MDB13
MAAB13	AR15	DDR1_MA14	DDR1_D14	AK32	MDB14
MAAB14	AV27	DDR1_MA15	DDR1_D15	AL32	MDB15
MAAB15	AY28	DDR1_MA16	DDR1_D16	AL34	MDB17
MODT_B0	AM17	DDR1_ODT0	DDR1_D17	AP34	MDB21
MODT_B1	AL18	DDR1_ODT1	DDR1_D18	AN31	MDB19
MODT_B2	AM16	DDR1_ODT2	DDR1_D19	AP31	MDB23
MODT_B3	AK15	DDR1_ODT3	DDR1_D20	AP35	MDB20
			DDR1_D21	AP35	MDB16
			DDR1_D22	AN32	MDB18
			DDR1_D23	AP32	MDB22
			DDR1_D24	AM29	MDB25
			DDR1_D25	AM28	MDB28
			DDR1_D26	AR29	MDB27
			DDR1_D27	AR28	MDB30
			DDR1_D28	AL28	MDB29
			DDR1_D29	AP29	MDB26
			DDR1_D30	AP28	MDB31
			DDR1_D31	AR12	MDB32
			DDR1_D32	AP12	MDB33
			DDR1_D33	AL13	MDB34
			DDR1_D34	AL12	MDB35
			DDR1_D35	AR13	MDB36
			DDR1_D36	AP13	MDB37
			DDR1_D37	AM13	MDB38
			DDR1_D38	AM12	MDB39
			DDR1_D39	AR9	MDB45
			DDR1_D40	AP9	MDB41
			DDR1_D41	AR6	MDB47
			DDR1_D42	AP6	MDB43
			DDR1_D43	AR10	MDB44
			DDR1_D44	AP10	MDB40
			DDR1_D45	AR7	MDB46
			DDR1_D46	AP7	MDB42
			DDR1_D47	AM9	MDB52
			DDR1_D48	AL9	MDB53
			DDR1_D49	AL6	MDB50
			DDR1_D50	AL7	MDB55
			DDR1_D51	AM10	MDB48
			DDR1_D52	AL10	MDB49
			DDR1_D53	AM6	MDB54
			DDR1_D54	AM2	MDB51
			DDR1_D55	AH6	MDB61
			DDR1_D56	AH7	MDB60
			DDR1_D57	AE6	MDB59
			DDR1_D58	AE7	MDB63
			DDR1_D59	AJ6	MDB56
			DDR1_D60	AJ7	MDB57
			DDR1_D61	AG6	MDB58
			DDR1_D62	AF7	MDB62
			DDR1_D63	AF35	DQSB0
			DDR1_D64	AL33	DQSB1
			DDR1_D65	AP33	DQSB2
			DDR1_D66	AN28	DQSB3
			DDR1_D67	AN12	DQSB4
			DDR1_D68	AP8	DQSB5
			DDR1_D69	AL8	DQSB6
			DDR1_D70	AG7	DQSB7
			DDR1_D71	AN25	DQSB0
			DDR1_D72	AK33	DQSB1
			DDR1_D73	AN33	DQSB2
			DDR1_D74	AN29	DQSB3
			DDR1_D75	AL13	DQSB4
			DDR1_D76	AR8	DQSB5
			DDR1_D77	AM8	DQSB6
			DDR1_D78	AG6	DQSB7
			DDR1_D79	AN26	

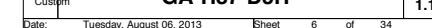
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LGA1150  
ILM\_BP/1156/BKN/[12KRC-0F0001-52R\_12KRC-0F0001-51R]

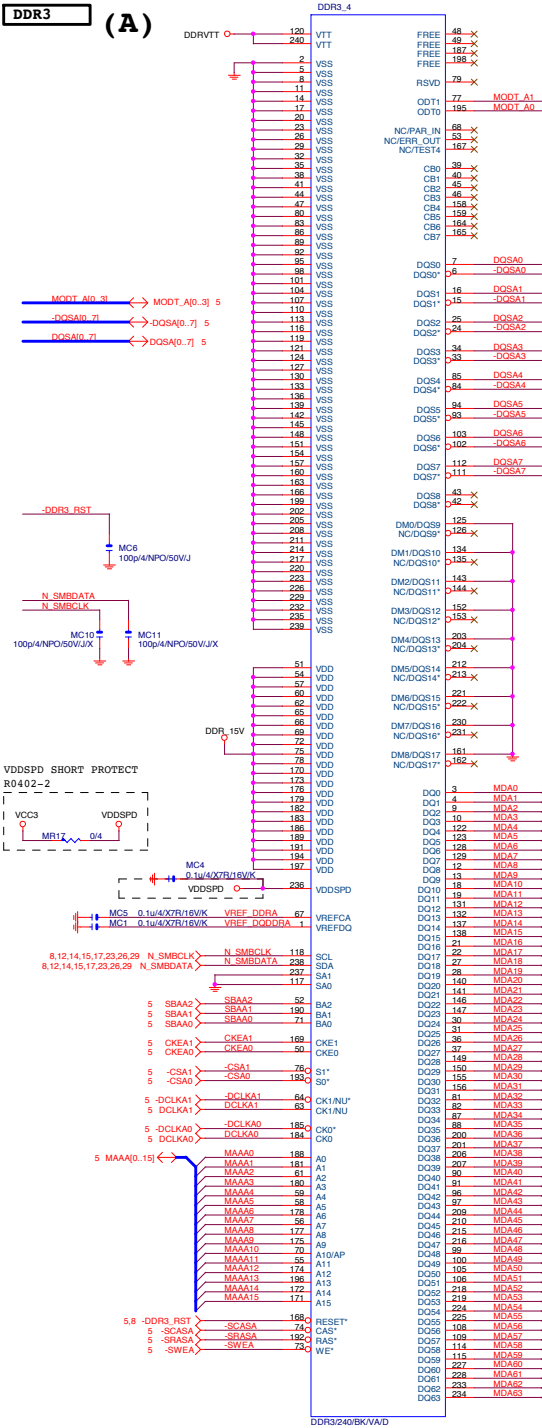
7 MODT_A[0..3]	MODT_A10..31
8 MODT_B[0..3]	MODT_B10..31
7 MDA[0..63]	MDA10..631
8 MDB[0..63]	MDB10..631
7 DQSA[0..7]	DQSA10..71
7 -DQSA[0..7]	-DQSA10..71
7 MAA[0..15]	MAA10..151
8 MAB[0..15]	MAB10..151
8 DQSB[0..7]	DQSB10..71
8 -DQSB[0..7]	-DQSB10..71



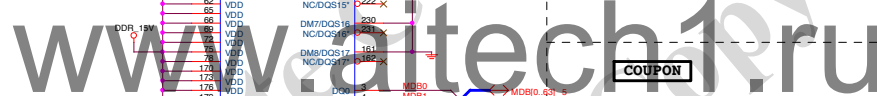
**(F, J)**









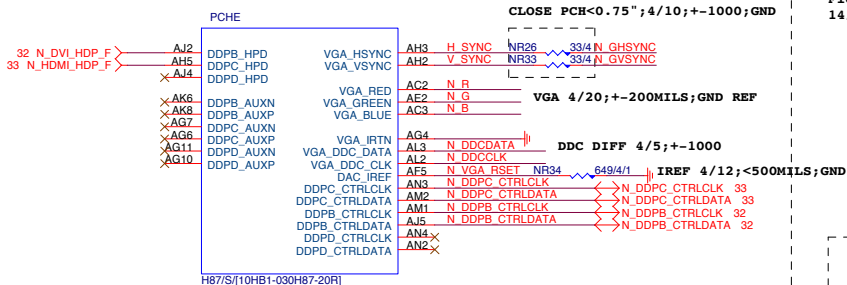






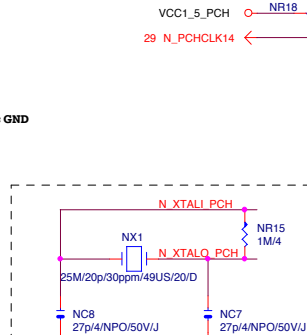


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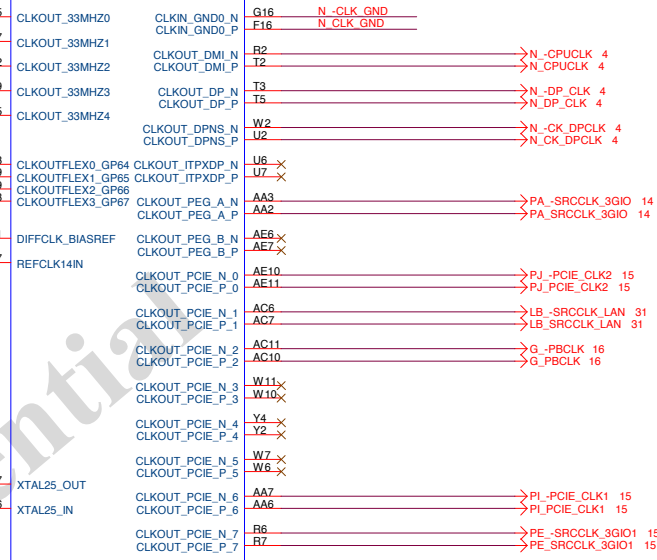


# PCH (G)

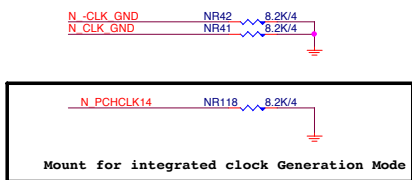
Flex1,2,3,4 : 14/24/33/48MHz



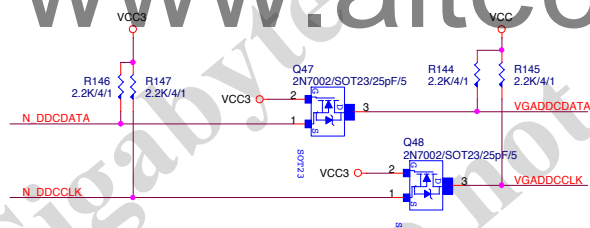
# PCHG



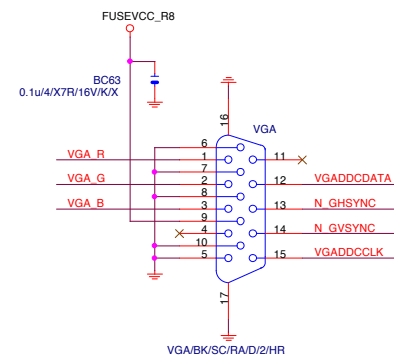
# PCH CLK PD



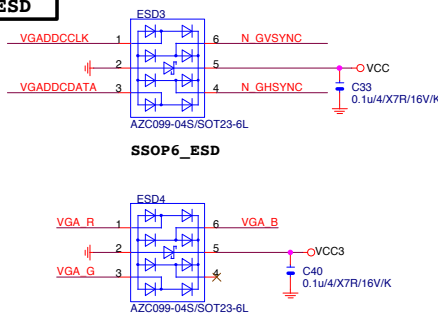
# VGA DDC



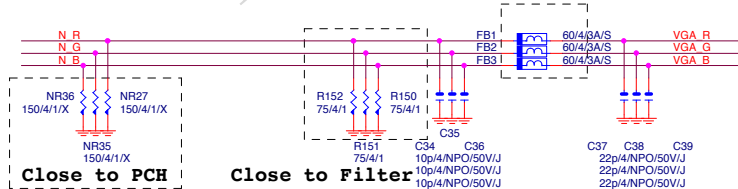
# VGA CONNECTOR



# VGA ESD



# VGA DDC



# Gigabyte Technology

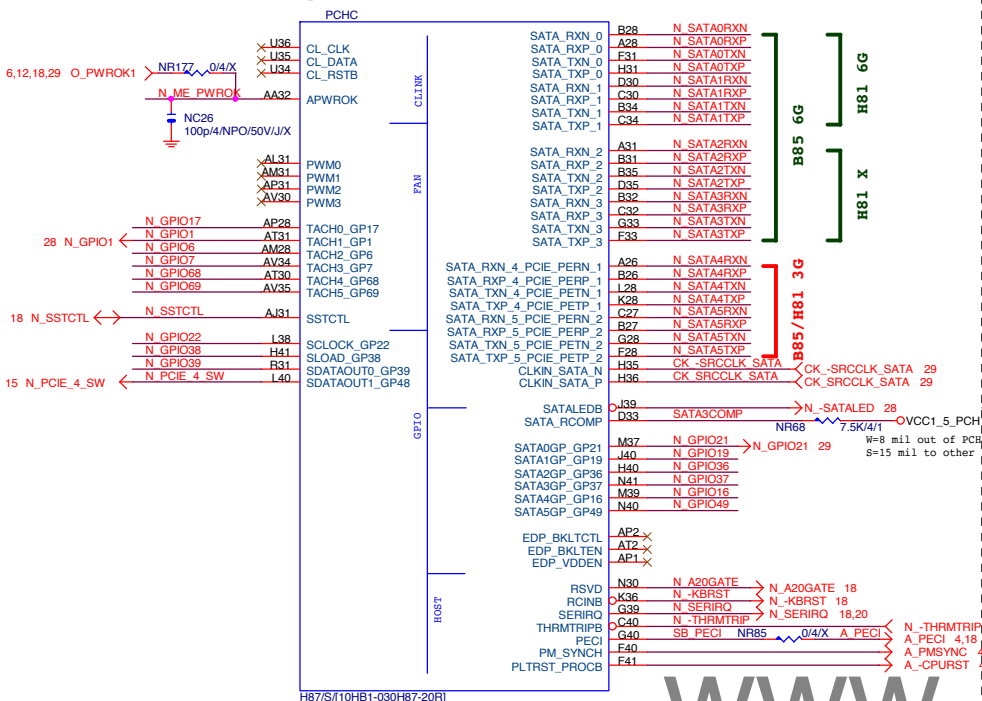
Title					PCH DISPLAY ,CLK BUFFER					
Size	Custom	Document Number				Rev 1:				
		GA-H87-D3H								
Date:		Tuesday, August 06, 2013			Sheet		10		of 34	



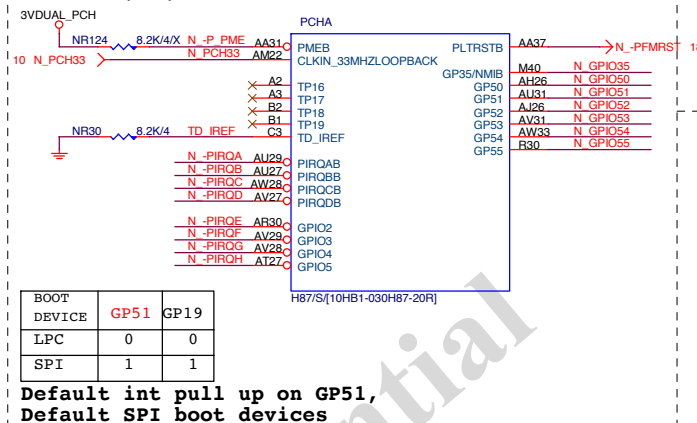
PCH

(C)

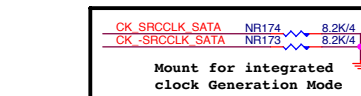
SATA3 : 20/4/4/20 (breakout min 8/4/4/8)  
Impedance=85 +/- 17.5%



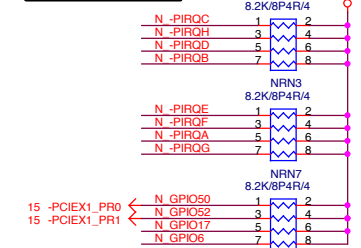
PCH (A)



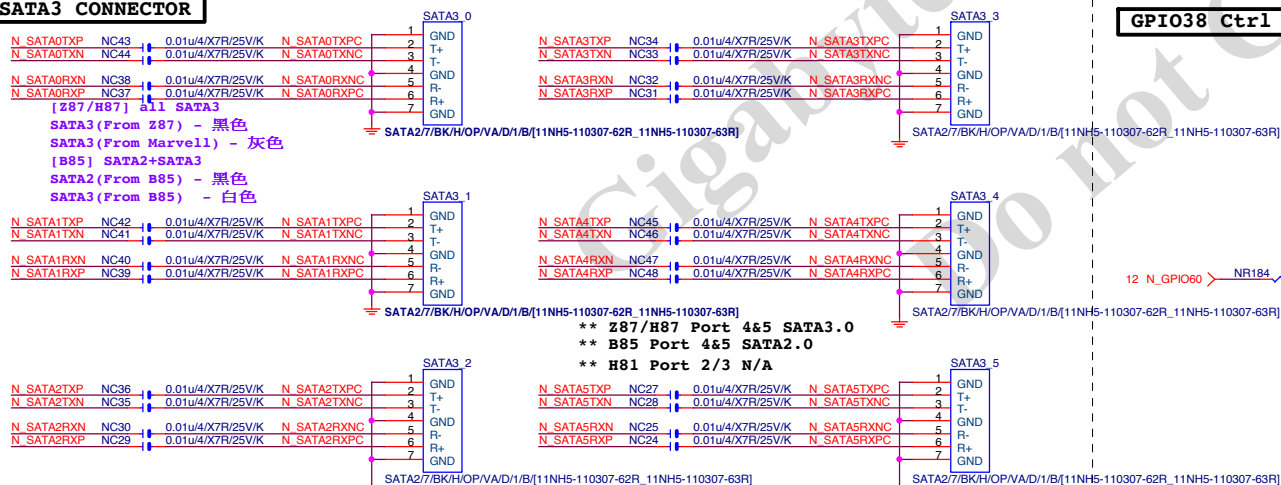
PCH CLK PD



PCH PU/PD



## SATA3 CONNECTOR



## GPIO38 Ctrl

MFG Mode  
N\_GPIO38 : Lo --> Enable  
Hi --> Disable

Gigabyte Technology

Title			PCH HOST , SATA, PCI	
Size	Document Number		Rev	
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(D)



```
C_ACZ_SDOUT : HI --> ME Enable
              Lo --> ME Disable
```



The schematic diagram shows the internal circuitry of the MMBT2222A/SOT23-600mA/A40 transistor. It includes a base-emitter junction (NR116) connected to the 3VDUAL\_PCH input, a base-collector junction (NR93), and a collector-emitter junction (NR253). The base is biased by a network of resistors (NC21, NR253, NR254) and capacitors (NR116, NR93). The emitter is connected to ground through a resistor (NR254). The collector is connected to the output terminal (NO3) through a resistor (NR253). The output terminal (NO3) is also connected to the output terminal (NO26) through a resistor (NR253).

GP44: BFX test Mode

NR139 8.2K/4/X N\_GPIO46

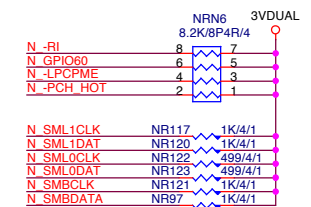
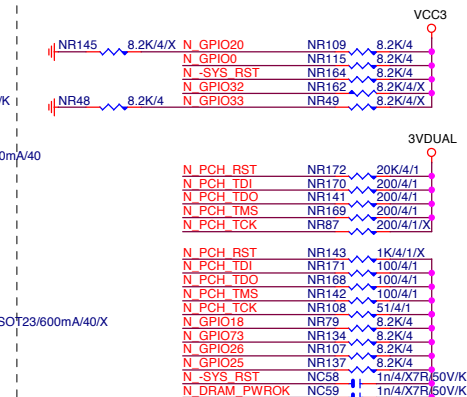
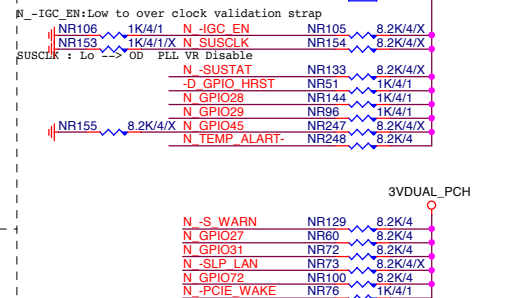
NR103 8.2K/4/X N\_GPIO44

N\_SKTOCC

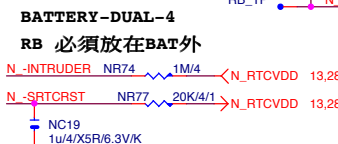
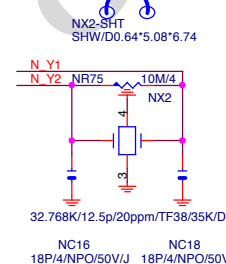
N\_GPIO57

3VDUAL

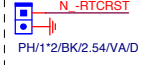
NRN9 8.2K/8P4/R4



32.768KHZ



CLR\_CMOS

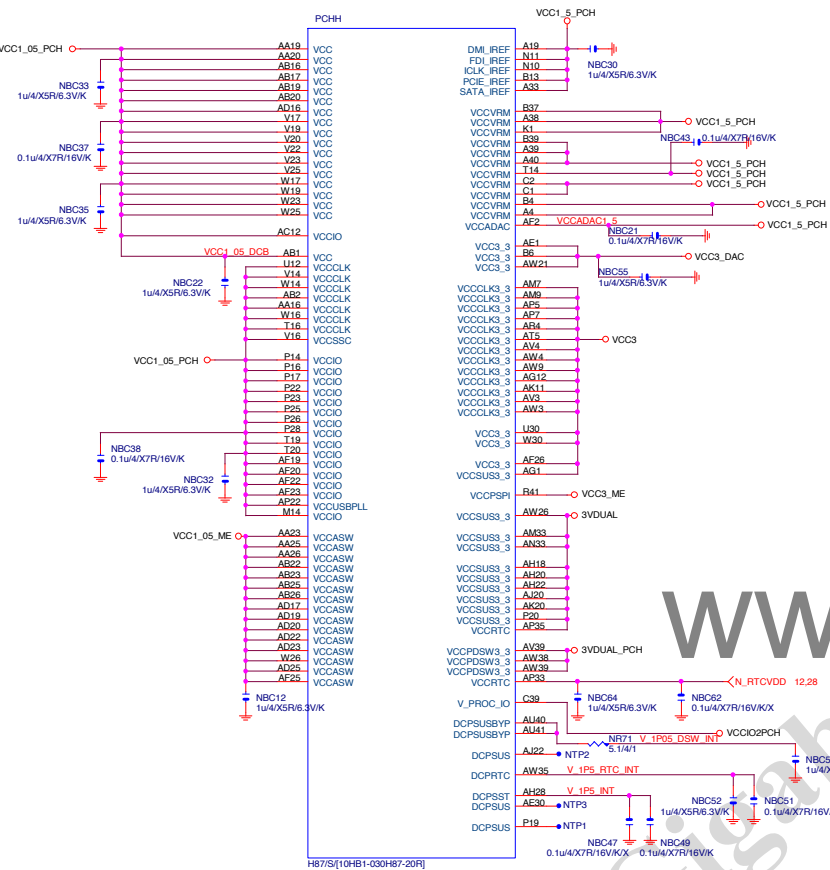


## Gigabyte Technology

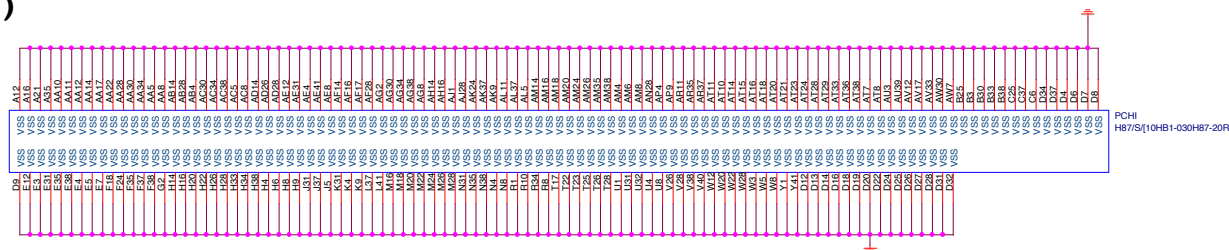
Title			
PCH GPIO , CTRL , AUDIO			
Size	Document Number	Rev	
Custom	GA-H87-D3H	1.1	
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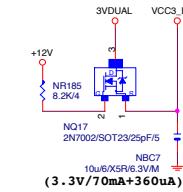
**(H)**



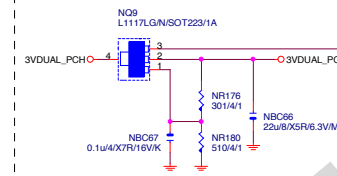
(I)



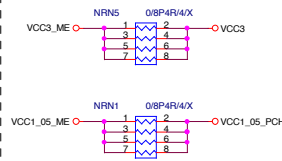
VCC3\_DAC



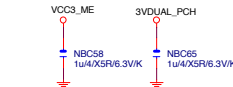
## 3VDUAL\_PCH



SHT PWR

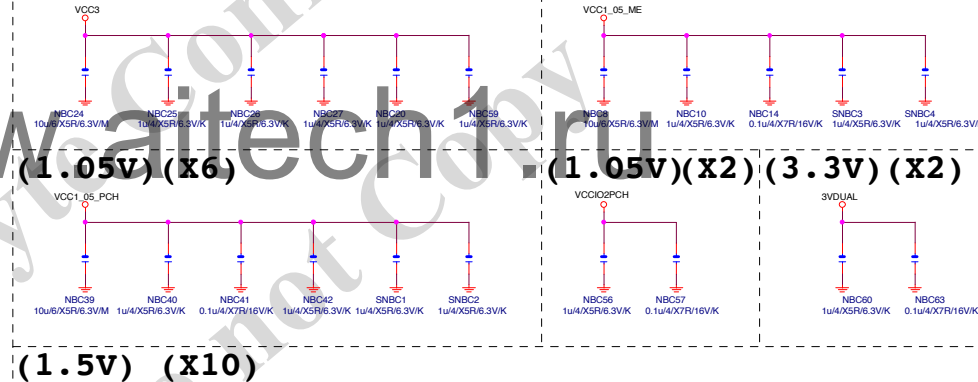


**CAP**



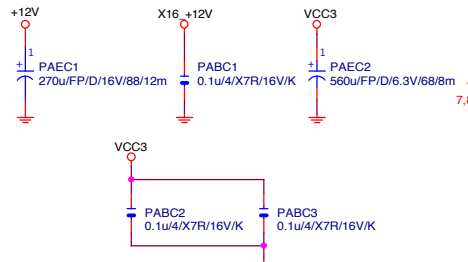
**(3.3V) (x6)**

(1.05V) (x5)



(1.5V) (x10)



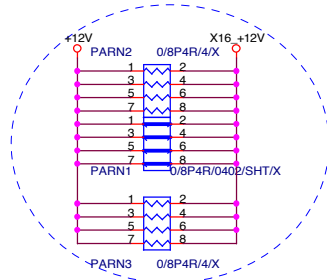
**PCIEX16 CAP**

PCIEX16	PROTECT	SHT
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```

+12 protect
short-wire test

```



PCIEX16 AC CAP

PA EXP TXP0	PAC5	0.22u4/X5R5/3V/K	PA EXP TXP0 C
PA EXP TXN0	PAC4	0.22u4/X5R5/3V/K	PA EXP TXN0 C
PA EXP TXM1	PAC6	0.22u4/X5R5/3V/K	PA EXP TXM1 C
PA EXP TXP1	PAC7	0.22u4/X5R5/3V/K	PA EXP TXP1 C
PA EXP TXP2	PAC8	0.22u4/X5R5/3V/K	PA EXP TXP2 C
PA EXP TXN2	PAC9	0.22u4/X5R5/3V/K	PA EXP TXN2 C
PA EXP TXP3	PAC10	0.22u4/X5R5/3V/K	PA EXP TXP3 C
PA EXP TXN3	PAC11	0.22u4/X5R5/3V/K	PA EXP TXN3 C
PA EXP TXP4	PAC12	0.22u4/X5R5/3V/K	PA EXP TXP4 C
PA EXP TXN4	PAC13	0.22u4/X5R5/3V/K	PA EXP TXN4 C
PA EXP TXP5	PAC14	0.22u4/X5R5/3V/K	PA EXP TXP5 C
PA EXP TXN5	PAC15	0.22u4/X5R5/3V/K	PA EXP TXN5 C
PA EXP TXP6	PAC16	0.22u4/X5R5/3V/K	PA EXP TXP6 C
PA EXP TXN6	PAC17	0.22u4/X5R5/3V/K	PA EXP TXN6 C
PA EXP TXP7	PAC18	0.22u4/X5R5/3V/K	PA EXP TXP7 C
PA EXP TXN7	PAC18	0.22u4/X5R5/3V/K	PA EXP TXN7 C
PA EXP TXP8	PAC20	0.22u4/X5R5/3V/K	PA EXP TXP8 C
PA EXP TXN8	PAC21	0.22u4/X5R5/3V/K	PA EXP TXN8 C
PA EXP TXP9	PAC22	0.22u4/X5R5/3V/K	PA EXP TXP9 C
PA EXP TXN9	PAC23	0.22u4/X5R5/3V/K	PA EXP TXN9 C
PA EXP TXP10	PAC24	0.22u4/X5R5/3V/K	PA EXP TXP10 C
PA EXP TXN10	PAC25	0.22u4/X5R5/3V/K	PA EXP TXN10 C
PA EXP TXP11	PAC26	0.22u4/X5R5/3V/K	PA EXP TXP11 C
PA EXP TXN11	PAC27	0.22u4/X5R5/3V/K	PA EXP TXN11 C
PA EXP TXP12	PAC28	0.22u4/X5R5/3V/K	PA EXP TXP12 C
PA EXP TXN12	PAC29	0.22u4/X5R5/3V/K	PA EXP TXN12 C
PA EXP TXP13	PAC30	0.22u4/X5R5/3V/K	PA EXP TXP13 C
PA EXP TXN13	PAC31	0.22u4/X5R5/3V/K	PA EXP TXN13 C
PA EXP TXP14	PAC32	0.22u4/X5R5/3V/K	PA EXP TXP14 C
PA EXP TXN14	PAC33	0.22u4/X5R5/3V/K	PA EXP TXN14 C
PA EXP TXP15	PAC34	0.22u4/X5R5/3V/K	PA EXP TXP15 C
PA EXP TXN15	PAC35	0.22u4/X5R5/3V/K	PA EXP TXN15 C

PCI-E REV:1.1--> 2.5GHZ

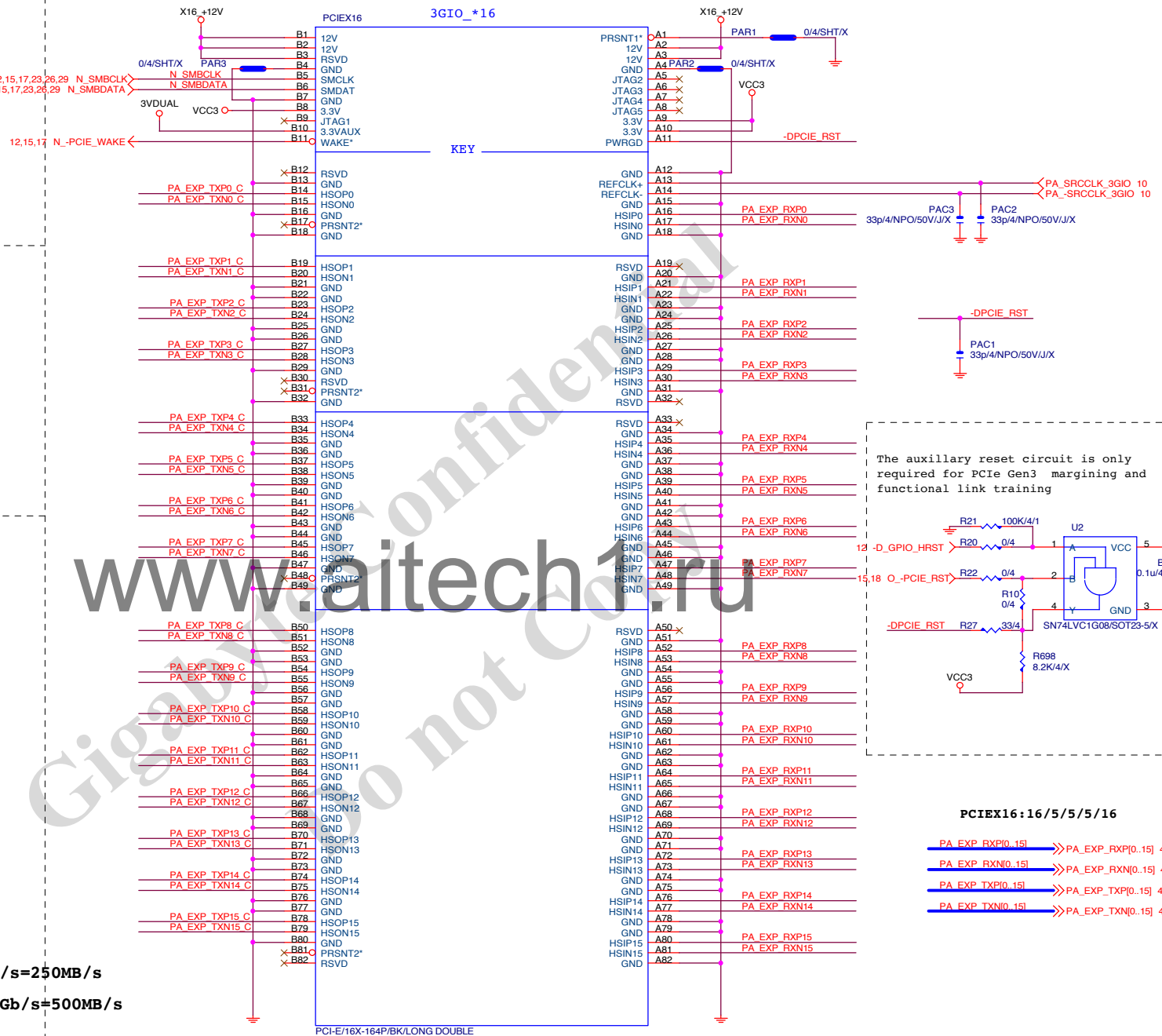
**PCE-E X1 (單向) BANDWIDTH=2.5GHz\*(8b/10b)=2Gb/s=250MB/s**

PCE-E X1(雙向) BANDWIDTH=2.5GHz\*(8b/10b)X2=4Gb/s=500MB/s

**PCE-E X16(單向) BANDWIDTH=2.5GHz\*(8b/10b)X16=32Gb/s=4GB/s**

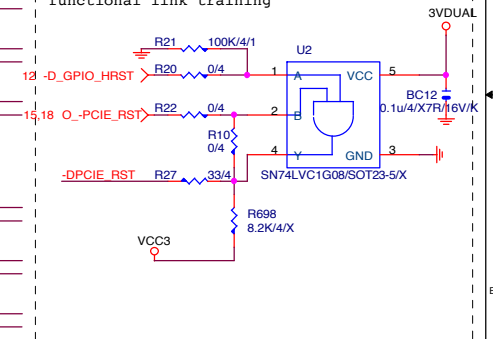
PCE-E X16(雙向) BANDWIDTH=2.5GHz\*(8b/10b)x16x2=64Gb/s=8GB/s

PCI-E REV:2.0--&gt; 5GHZ

**PCIEX16 SLOT****PCIESLOT-164DN-Q**

PCI-E/16X-164P/BK/LONG DOUBLE

The auxillary reset circuit is only required for PCIe Gen3 margining and functional link training



PCIEX16:16/5/5/5/16

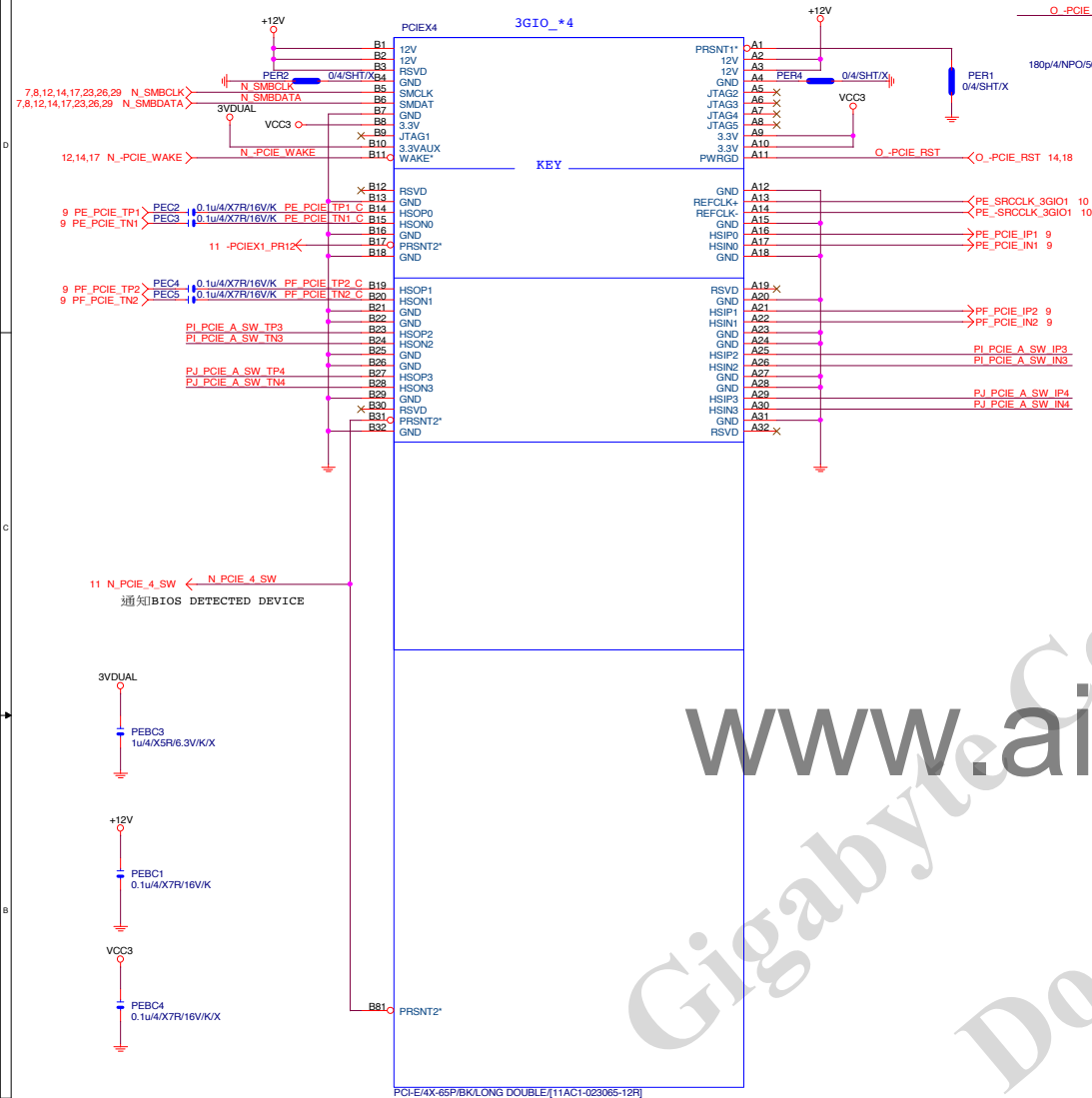
<u>PA EXP RXP[0..15]</u>	<u>&gt;&gt;&gt;PA_EXP_RXP[0..15]</u>	4
<u>PA EXP RXN[0..15]</u>	<u>&gt;&gt;&gt;PA_EXP_RXN[0..15]</u>	4
<u>PA EXP TXP[0..15]</u>	<u>&gt;&gt;&gt;PA_EXP_TXP[0..15]</u>	4
<u>PA EXP TXN[0..15]</u>	<u>&gt;&gt;&gt;PA_EXP_TXN[0..15]</u>	4

## Gigabyte Technology

Title			
PCI EXPRESS * 16			
Size	Document Number		Rev
Custom	GA-H87-D3H		1.1
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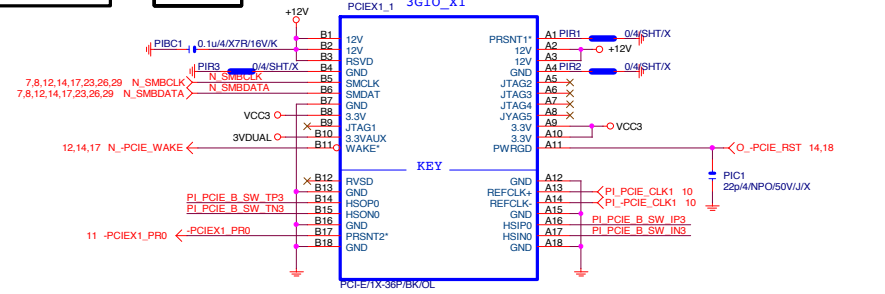
# PCIEX4 SLOT



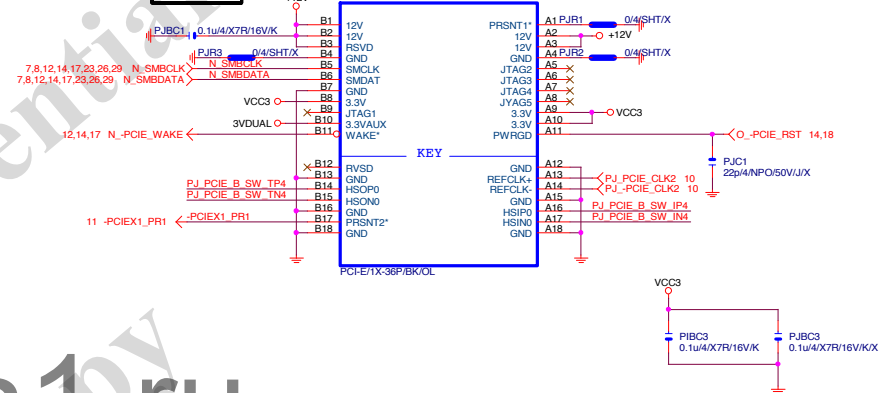
	N PCIE 4 SW (PCH GPIO48)	PCIEX4 X1 (SIO GPIO26)
P	H	H
PCIEX4 No devices	H	H
PCIEX4 -> X1	H	H
PCIEX4 Have devices	L	L
PCIEX4 -> X4	L	L
PCIEX1_1/2 --> N/A		

# PCIEX1 SLOT

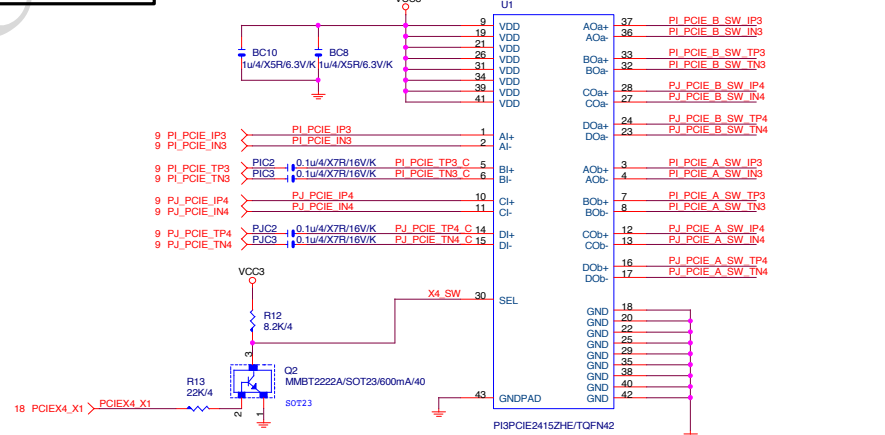
# PCIEX1\_1



# PCIEX1\_2



# PCIEX4/X1 SWITCH

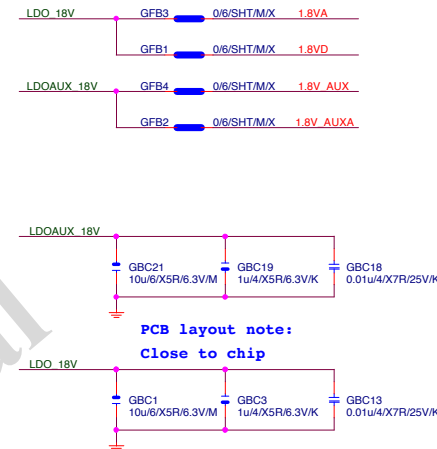


Function	SEL
x1--> x0a	L;PCIEX4 SLOT-->X1
x1--> x0b	H;PCIEX4 SLOT-->X4

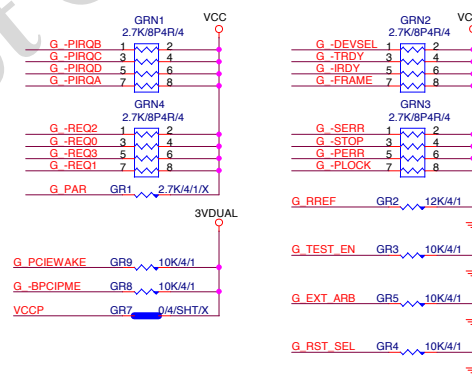
# Gigabyte Technology

Title	PCIE X1 1,2		
Size	Document Number	GA-H87-D3H	Rev 1.1
Date:	Tuesday, August 06, 2013	Sheet 15	of 34

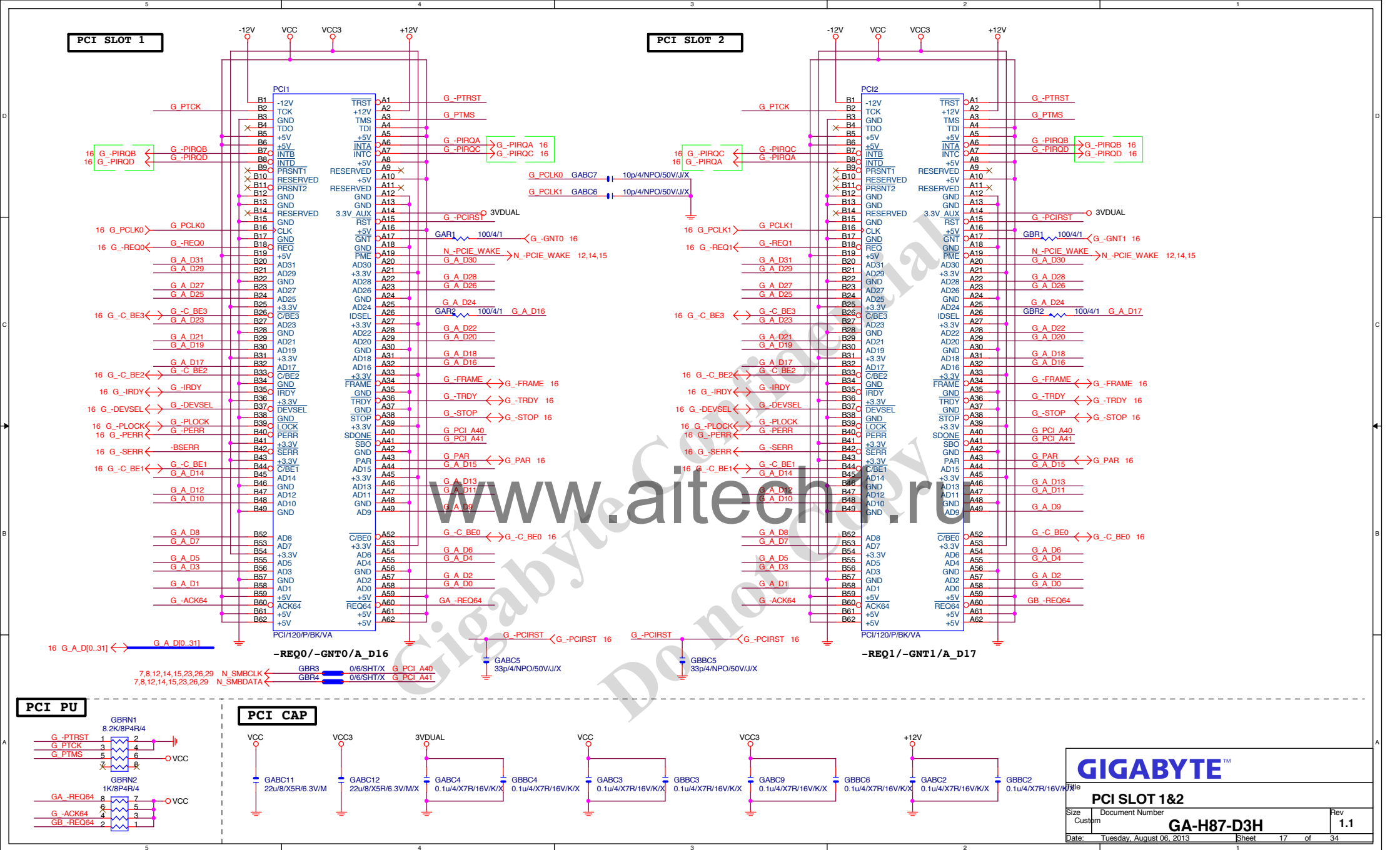




High: PCICLK INPUT form CLK Gen  
Low: PCICLK OUTPUT form IT8893 chip

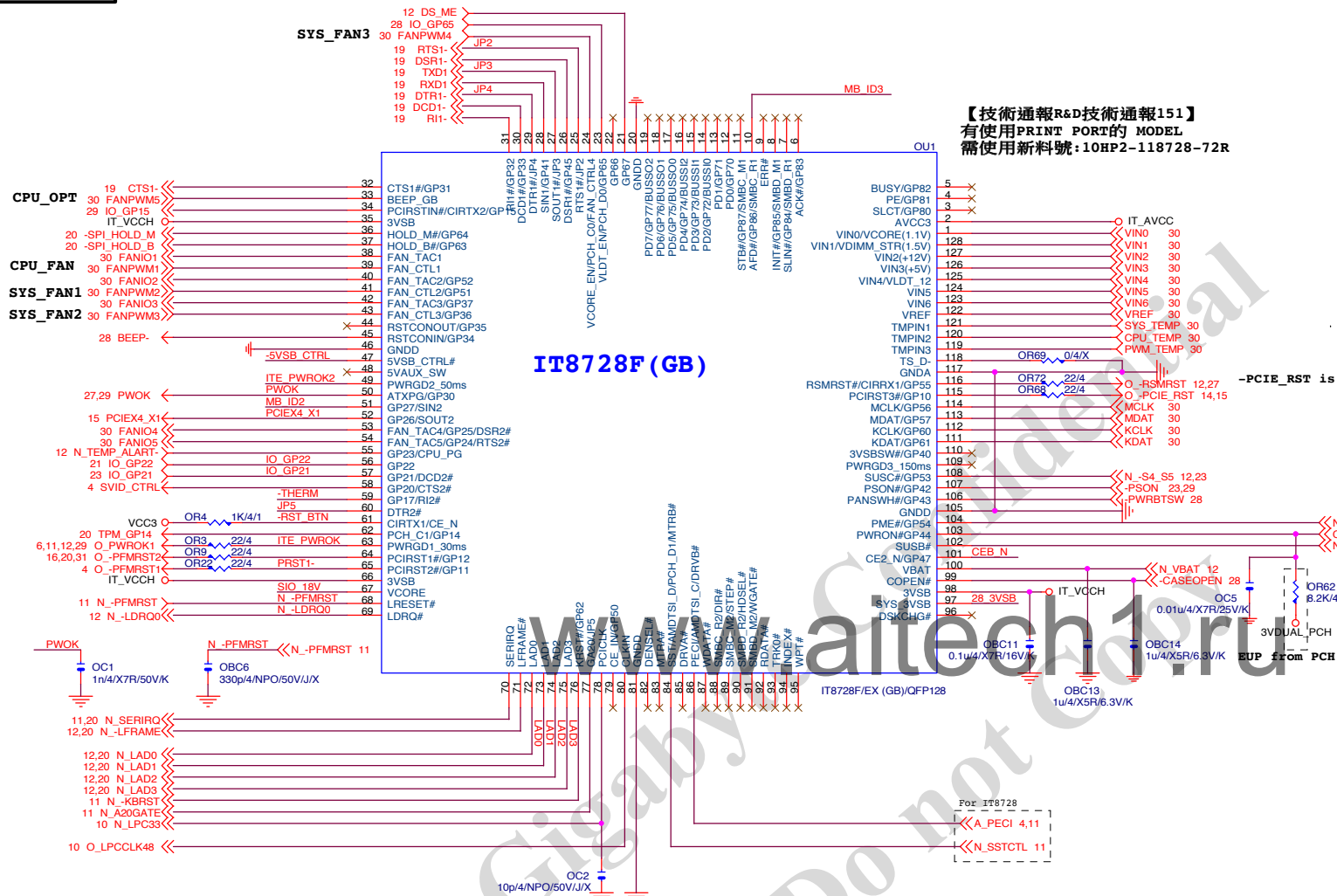








**SIO IT8728F**



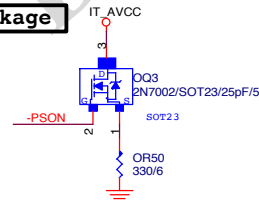
## IT8728F NOTE

	<b>IT8728</b>
<b>PIN121</b>	<b>VCORE_EN/PCH_C0</b>
<b>PIN120</b>	<b>VLD2_EN/PCH_D0</b>
<b>PIN19</b>	<b>ATXPG</b>
<b>PIN31</b>	<b>PCH_C1</b>
<b>PIN53</b>	<b>SST/AMDTSI_D/MTRB#/PCH_D1</b>
<b>PIN55</b>	<b>PECI/AMDTSI_C/DRV#</b>
<b>PIN66</b>	<b>SYS_3VSB</b>
<b>PIN70</b>	<b>GP47</b>
<b>PIN95</b>	<b>VIN2(VCC5)</b>
<b>PIN96</b>	<b>VIN1(VCC12)</b>
<b>PIN97</b>	<b>VIN1/VDIMM_STR(1.5V)</b>
<b>PIN98</b>	<b>VIN0/VCORE(1.1V)/NC</b>

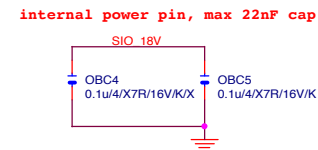
**DUAL BIOS OPT STRAP**



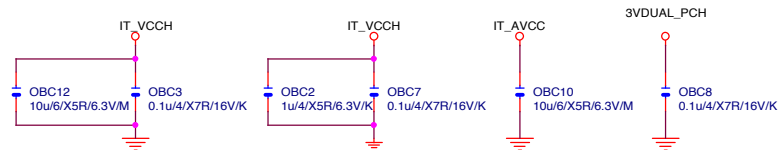
## Power leakage



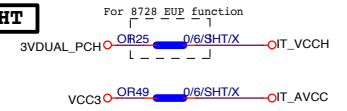
SIO 18V



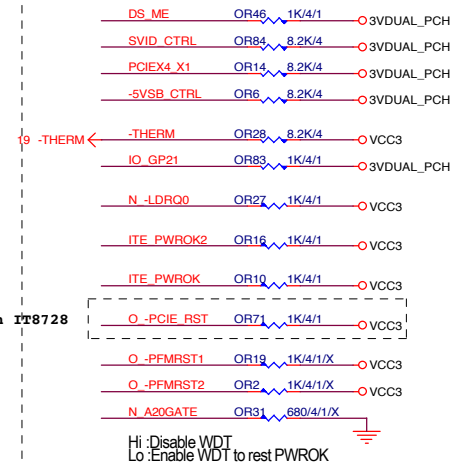
SIO CAP



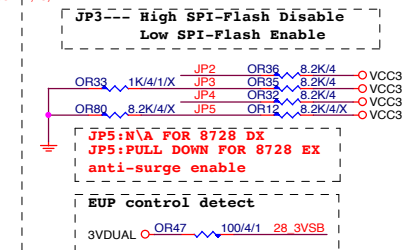
**PWR SHT**



**SIO PU**

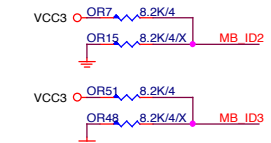


**SIO STRAP**



JP4	1	k8 power sequency function is Disable
	0	k8 power sequency function is Enable
JP3	1 1	The default value of EC Index 63h/6Bh/73h is 80h.
	1 0	The default value of EC Index 63h/6Bh/73h is FFh.
JP5	0 1	The default value of EC Index 63h/6Bh/73h is 00h.
	0 0	The default value of EC Index 63h/6Bh/73h is 40h.

MB ID

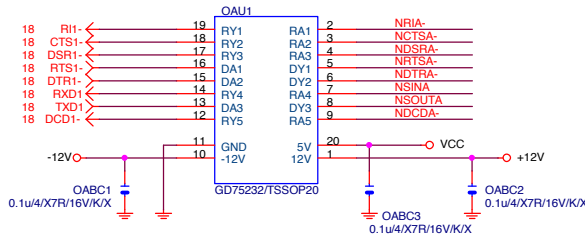


## Gigabyte Technology

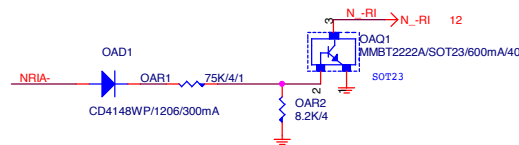
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ITE 8728 LPC IO			
Size B	Document Number		Rev 1.1
GA-H87-D3H			
Date:	Tuesday, August 06, 2013	Sheet	18 of 34



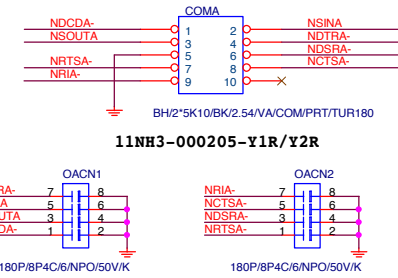
## COMA



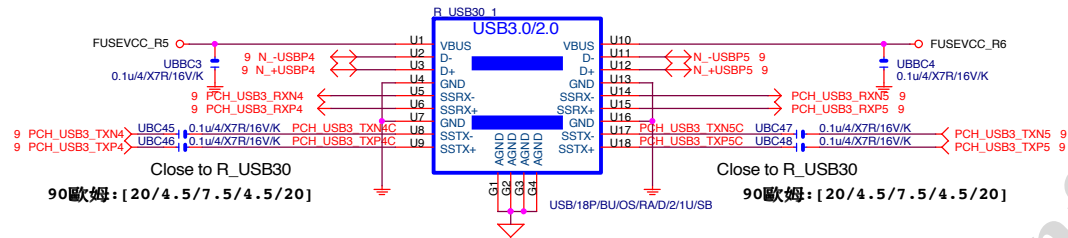
## COM RI



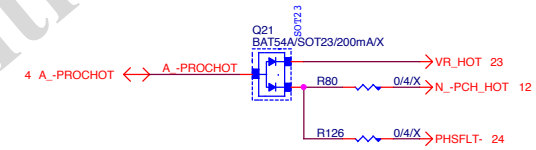
## COM BUFFER



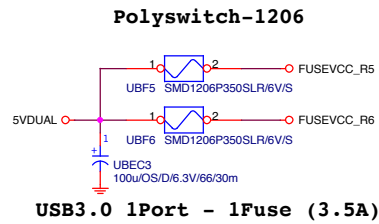
## USB30\_20 CONNECT



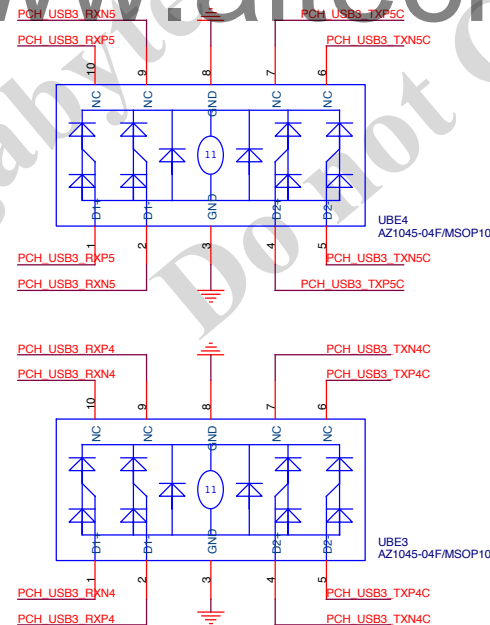
## -PROHOT



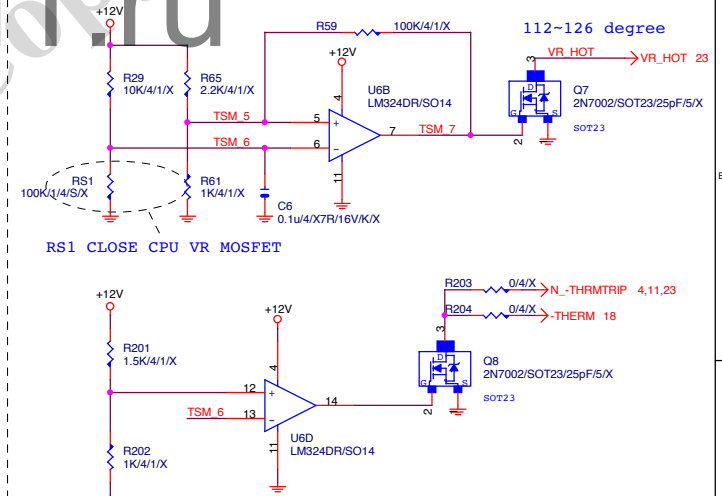
## USB30 PWR



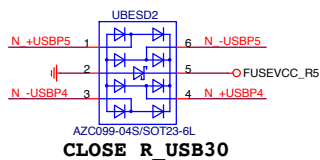
## USB30 ESD PROTECT



## -PROHOT



## USB20 ESD PROTECT



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Title	COM & PROHOT/Dynamic O.C.		
Size	Document Number	Rev	1.1
Custom	GA-H87-D3H		
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## DUAL BIOS

## MOSI For DMI RX Termination Voltage

12 N_ICH_SPI_MOSI	N_ICH_SPI_MOSI	NR10	8.2K/4/X
12 N_ICH_SPI_CS	N_ICH_SPI_CS	NR9	8.2K/4/X
12 N_ICH_SPI_CS1	N_ICH_SPI_CS1	NR246	8.2K/4/X
18 -SPI_HOLD_M	-SPI_HOLD_M	NR3	1K/4/1
18 -SPI_HOLD_B	-SPI_HOLD_B	NR11	1K/4/1

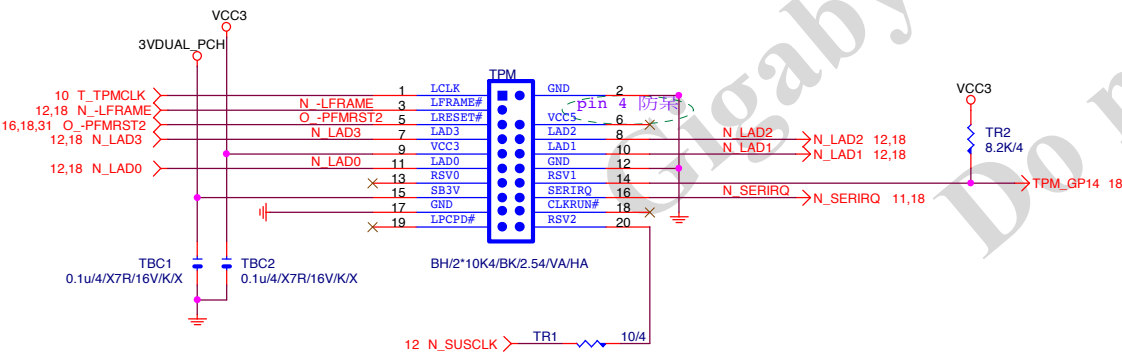
N -SPI_WP1	NR2	8.2K/4/X
N -SPI_WP0	NR1	8.2K/4/X
N_ICH_SPI_MISO	NR5	8.2K/4
-HOLD0	NR235	1K/4/1/X
-HOLD1	NR236	1K/4/1/X

18 -SPI_HOLD_M	-SPI_HOLD_M	NR237	1K/4/1/X
18 -SPI_HOLD_B	-SPI_HOLD_B	NR238	1K/4/1/X
12 N_ICH_SPI_MISO		NR6	22/4

BOOT DEVICE	GNT0	GNT1
LPC	0	0
PCI	0	1
NAND	1	0
SPI	1	1

1 means floating  
0 means PD 1K

## TPM CONNECT

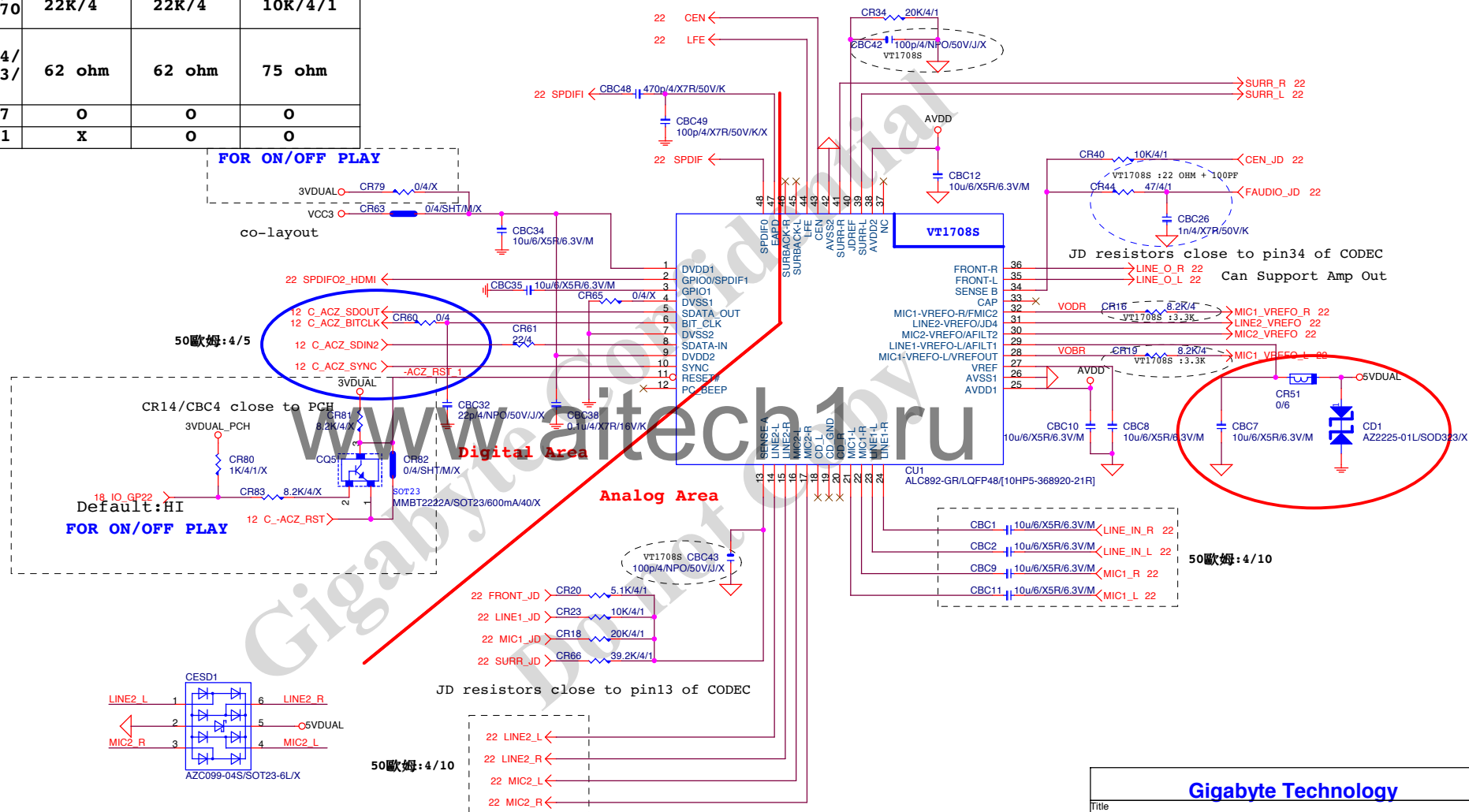


Gigabyte Technology

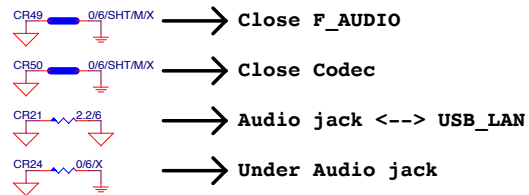
Title			BIOS
Size	Document Number	GA-H87-D3H	
Custom		Rev	1.1
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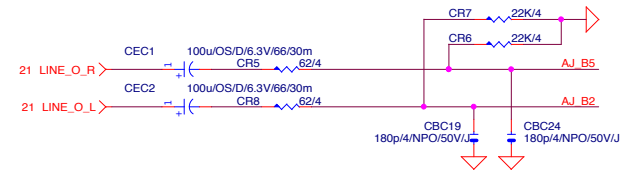
	ALC892	ALC887-VD2	VT1708S-CE
CR44/CBC26	47ohm+1nF	47ohm+1nF	22ohm+100P
CBC42/CBC43	X	X	100P/4
CR16/CR19 CR52/CR56/CR10/CR9	8.2K/4	8.2K/4	3.3K/4/1
CR6/CR7/CR58/CR54/ CR67/CR68/CR69/CR70	22K/4	22K/4	10K/4/1
CR5/CR8/CR1/CR14/ CR17/CR22/CR73/CR74/ CR13/CR11/CR57/CR53/ CR75/CR76	62 ohm	62 ohm	75 ohm
CR51/CD1/CBC7	O	O	O
CESD1	X	O	O





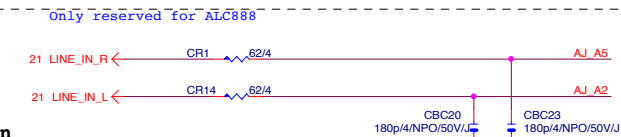


## LINE-OUT



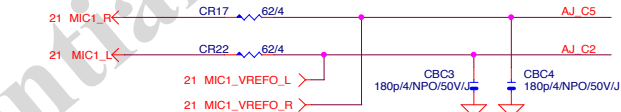
## LINE-IN

Verify MIC function in LINE-in

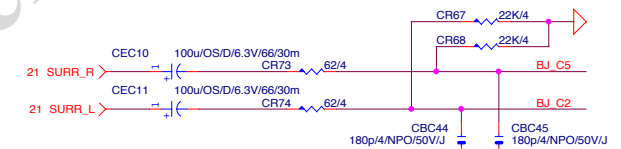


For 889A/888

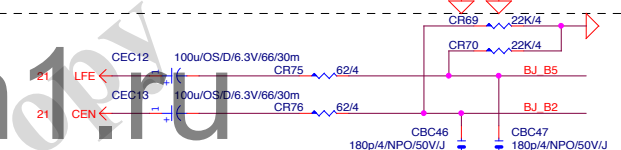
## MIC-IN



## SURROUND

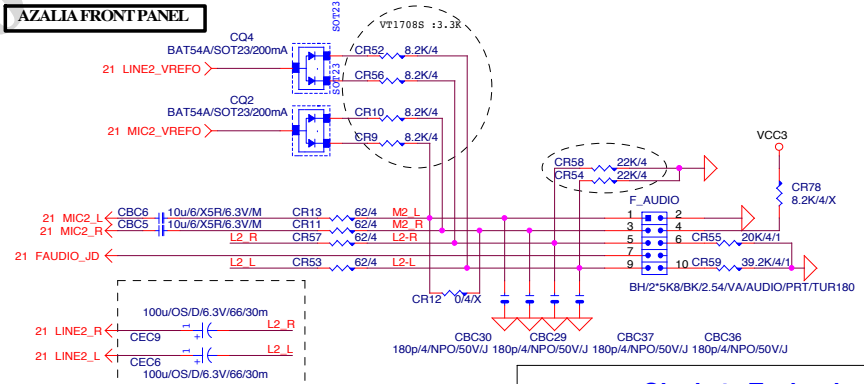


## CEN/LFE



## SURRBACK

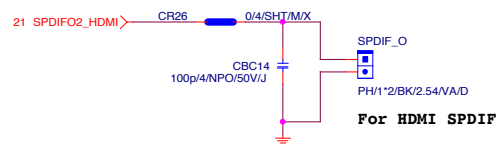
## AZALIA FRONT PANEL



Gigabyte Technology

Title			
AUDIO JACK			
Size	Document Number	Rev	
Custom	GA-H87-D3H	1.1	
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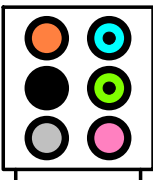
## SPDIF\_OUT



## SPDIF\_IN



## AZALIA JACK



## AZALIA JACK

BLUE LINE-IN

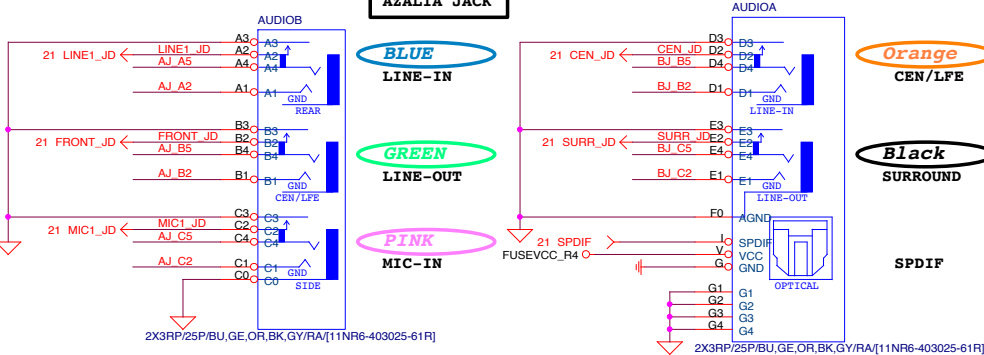
GREEN LINE-OUT

PINK MIC-IN

Orange CEN/LFE

Black SURROUND

SPDIF





Value need check with Vendor

Close to DDR  
output inductor  
ML1

should be routed as  
differential pair,  
7mil width,8mil  
spacing

need 0.1amp , check trace width

Close DDR3 SLOT

To CPU pin AB3,AB4

Debug Port

To system SMBUS

To CPU side SVID Bus

Close to Vcore  
output inductor  
DA\_DL1

should be routed as  
differential pair,  
7mil width,8mil  
spacing

Value need check with Vendor

should be routed as  
differential pair,  
7mil width,8mil  
spacing

Close to  
Vcore MOS  
DB\_DU1

For VTT\_PWRGD sequency

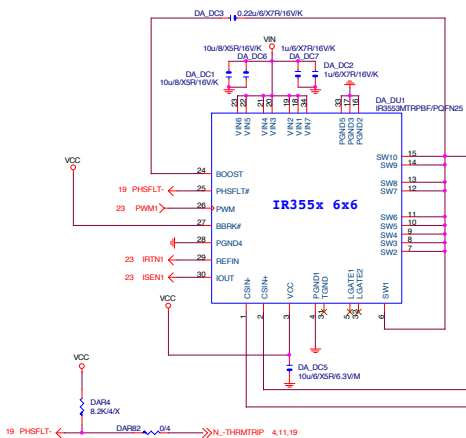
For DDR\_15V dummy load

DDR\_VTT

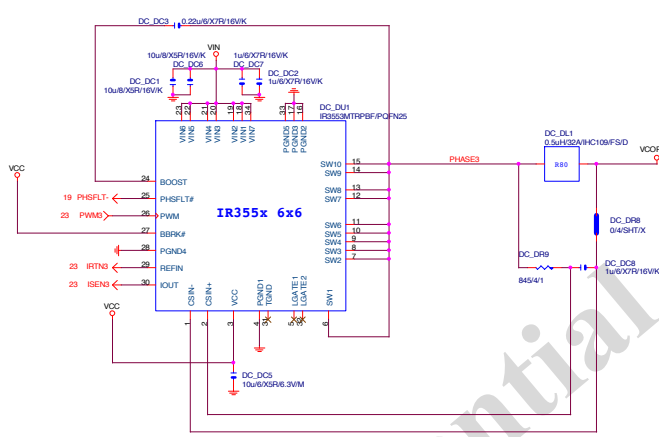


## VCORE

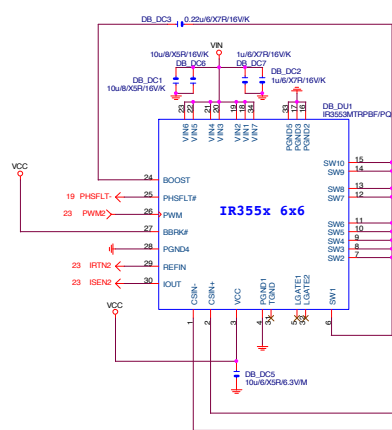
## VCORE-PHASE1



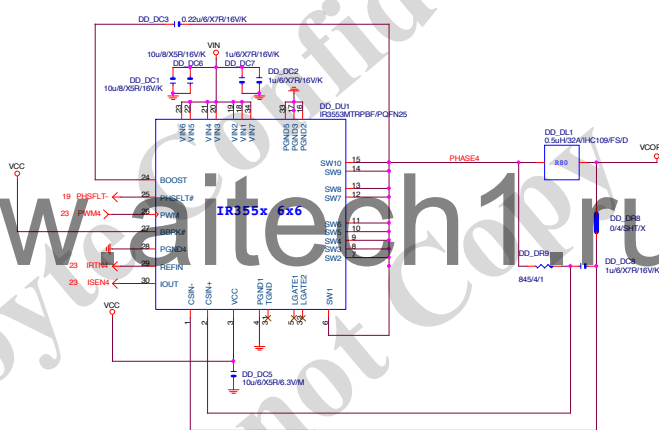
## VCORE-PHASE3



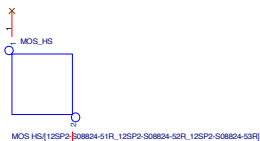
## VCORE-PHASE2



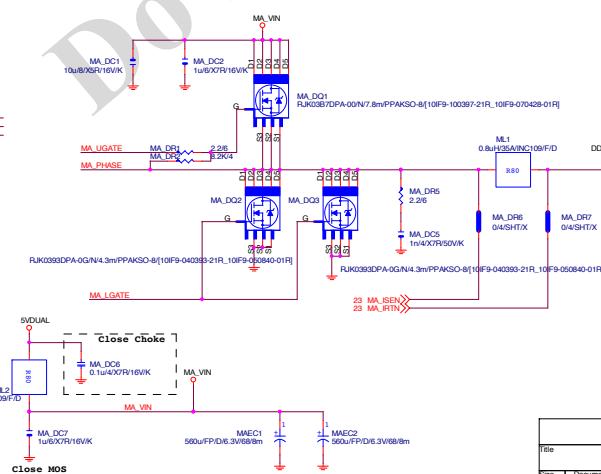
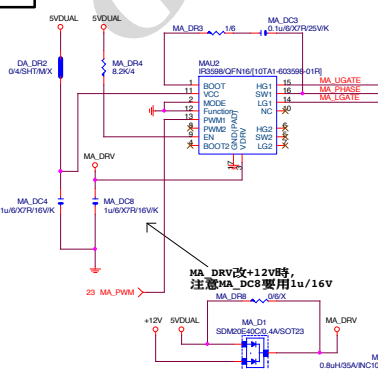
## VCORE-PHASE4



## MOSFET HEATSINK



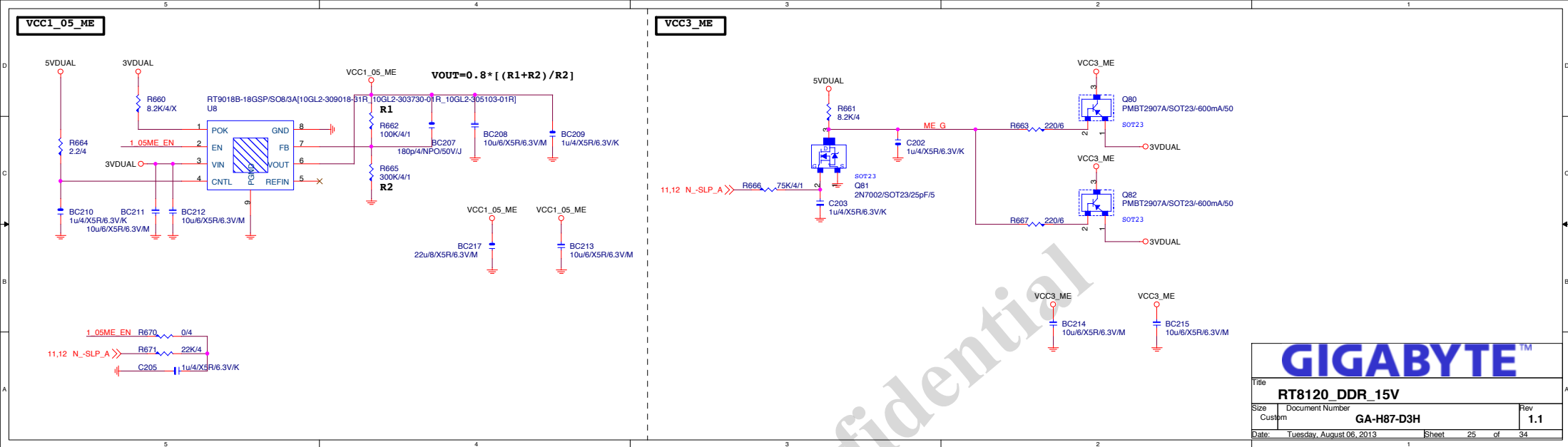
## DDR\_15V



FUNCTION	MODE	PWM MODE	PHASE MODE
0	1	IR ATL	DUAL
1	1	IR ATL	Doubler
0	0	Tri-Steate	DUAL
1	0	Tri-Steate	Doubler
OPEN	0	Tri-Steate	Quad
OPEN	1	IR ATL	Quad

In Quad mode , IC1 pin10 link to IC2 pin10  
IC1 pin9 link to IC2 pin9 without PU

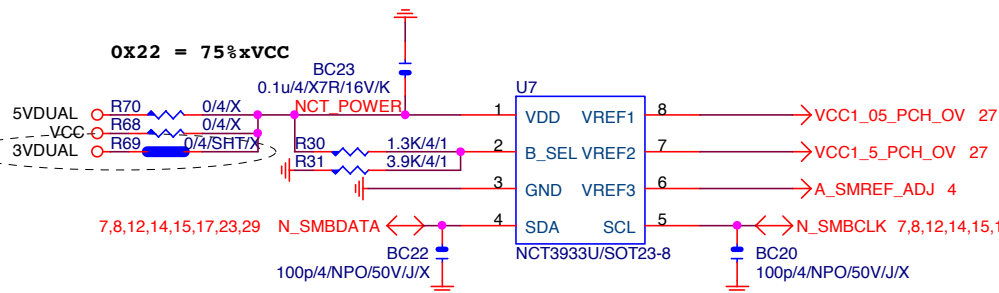




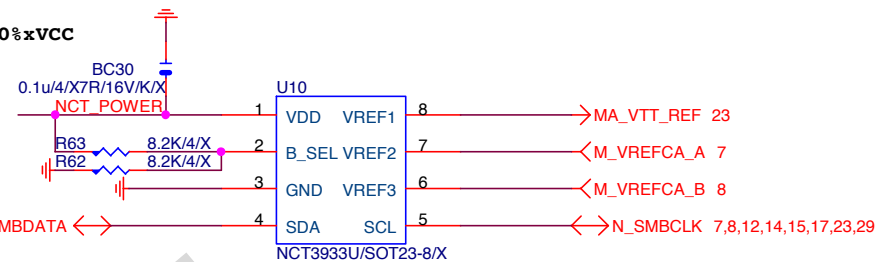
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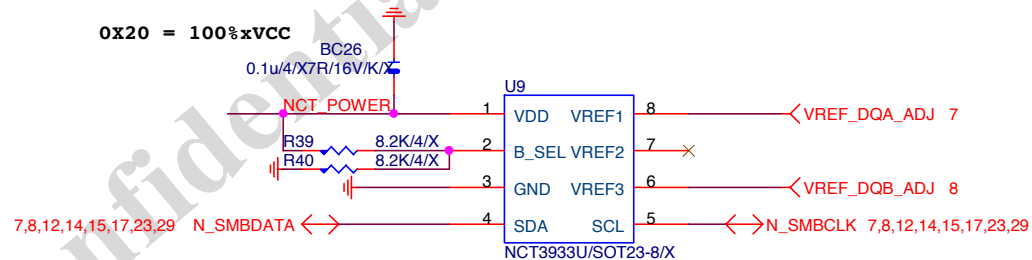
# OVER VOLTAGE



**0X2A = 0%xVCC**



**0X20 = 100%xVCC**



NCT3933	0X2A	0X20	0X22
VREF1	DDRVTT	VREF_DDRA_DQ	PCH Core
VREF2	VREF_DDRA_CA	N/A	VCC1_5_PCH
VREF3	VREF_DDRA_CA	VREF_DDRB_DQ	SMREF

**Gigabyte Technology**

**CPU CORE VR-2**

**GA-H87-D3H**

Size	Document Number	Rev
Custom		1.1

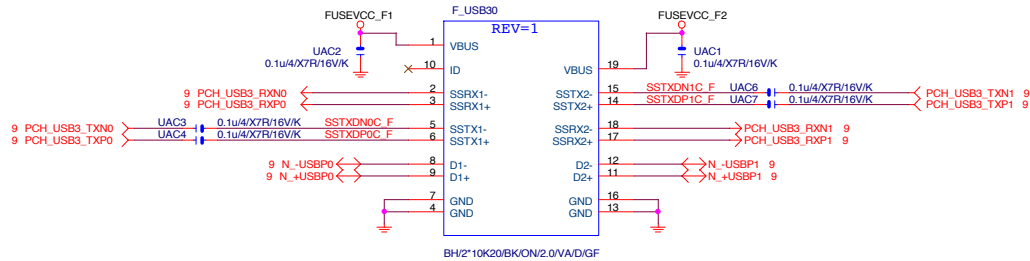
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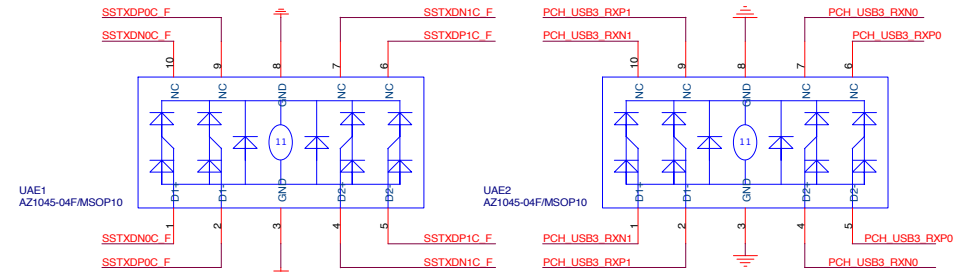




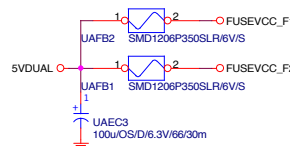
# Front USB3.0



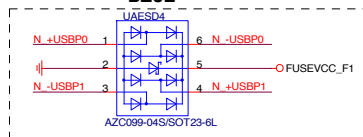
# F\_USB30 ESD PROTECT



# F\_USB30 PWR

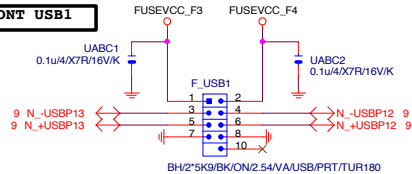


# BLUE

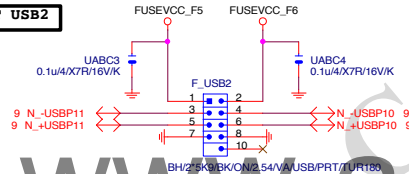


Close to connector

# FRONT USB1

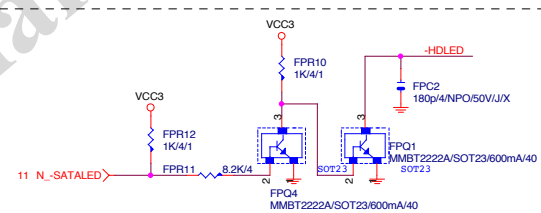


# FRONT USB2

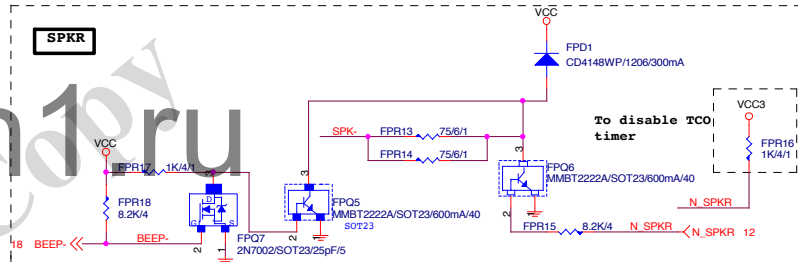


Close to connector

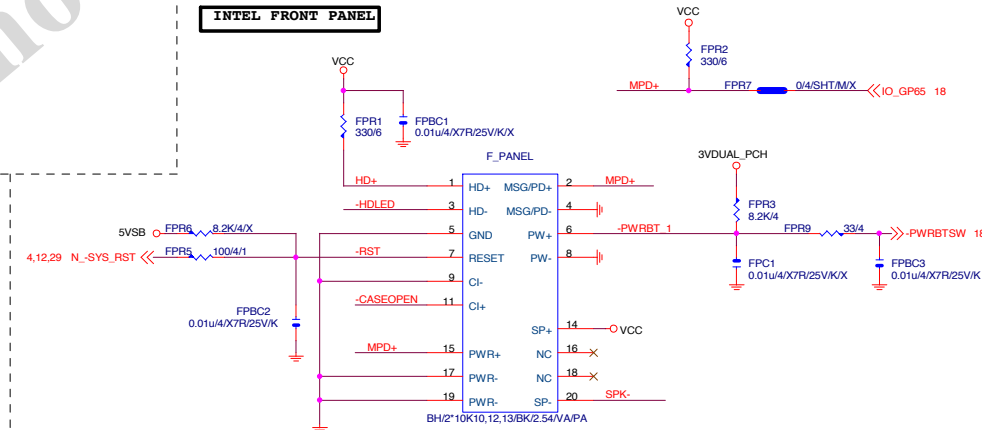
# SATA\_LED



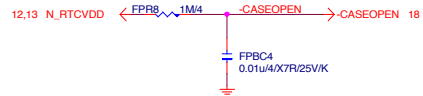
# SPKR



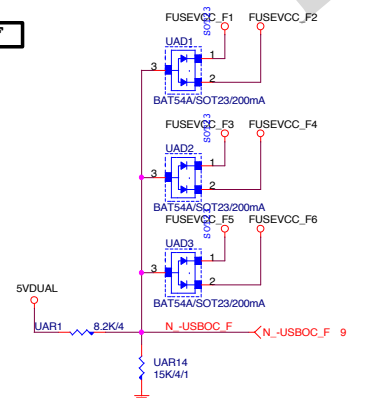
# INTEL FRONT PANEL



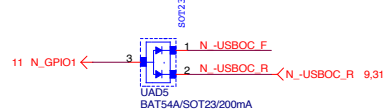
# CASE OPEN



# -USBOC\_F



# F\_USB POWER PROTECT



Gigabyte Technology

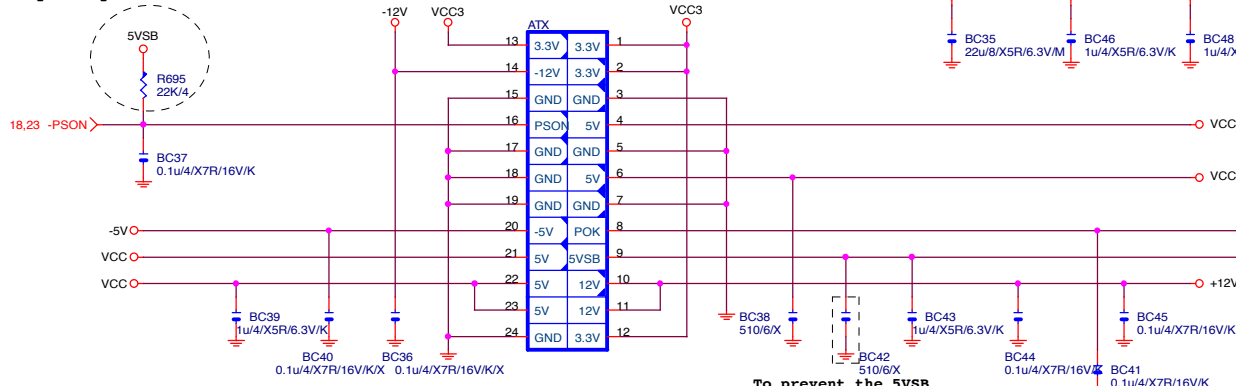
FP,F\_USB,USB PWR,FDD,BZ

GA-H87-D3H

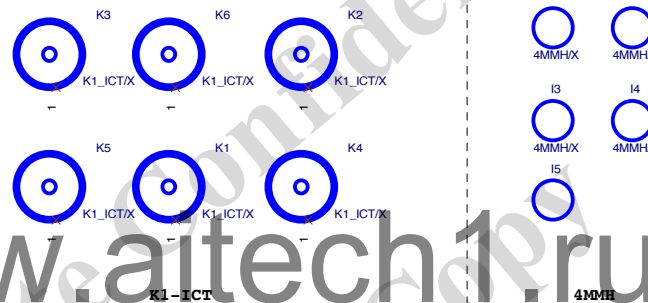
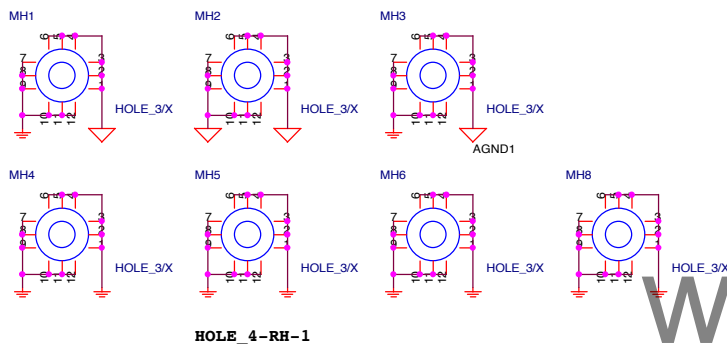
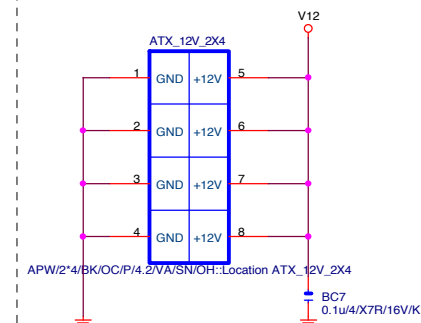
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Size	Custom	1.1
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Patch some PSU no internal pull up resistor

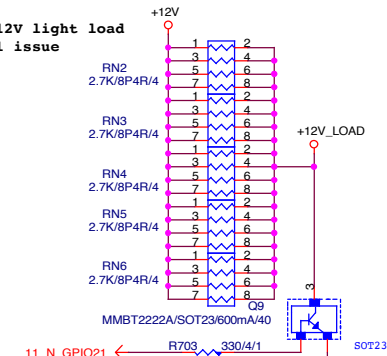


## ATXX4 POWER CONNECTOR



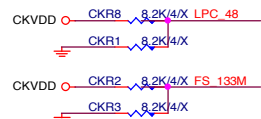
## 【技術通報R&D技術通報153】

To fix 12V light load abnormal issue

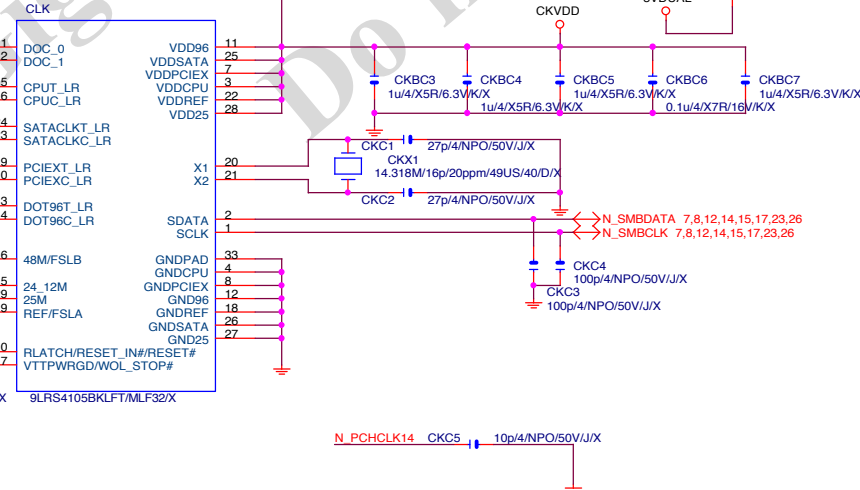
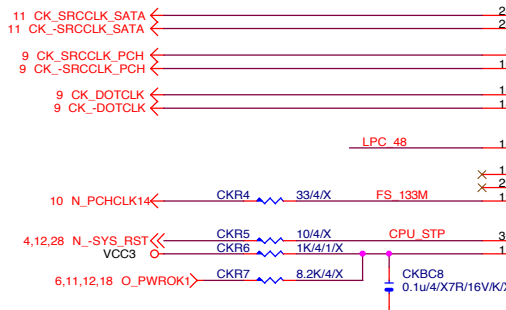


## CLK GEN

### CPU Frequency Selection

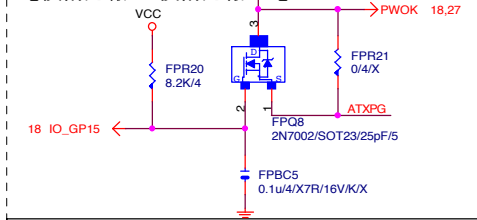


FSLB	FSLA	CPU
0	0	100M <Default>
0	1	133M
1	0	200M
1	1	166M



## PWOK PATCH

### 【技術通報R&D技術通報154】

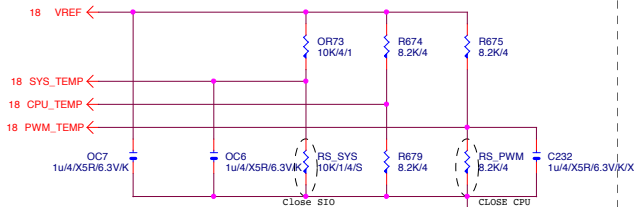


Gigabyte Technology

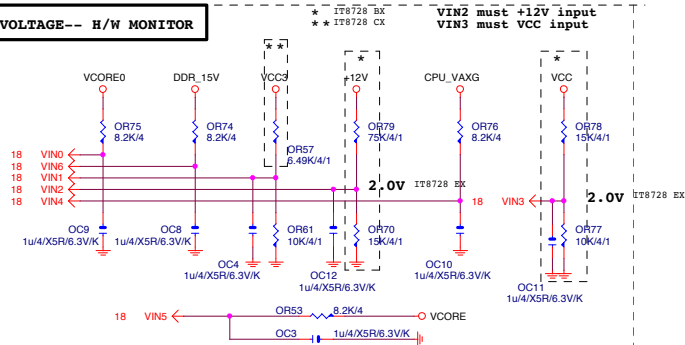
Title		ATX POWER CONNECTOR	
Size	Document Number	GA-H87-D3H	
Custom		Rev 1.1	
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## TEMP H/W MONITOR

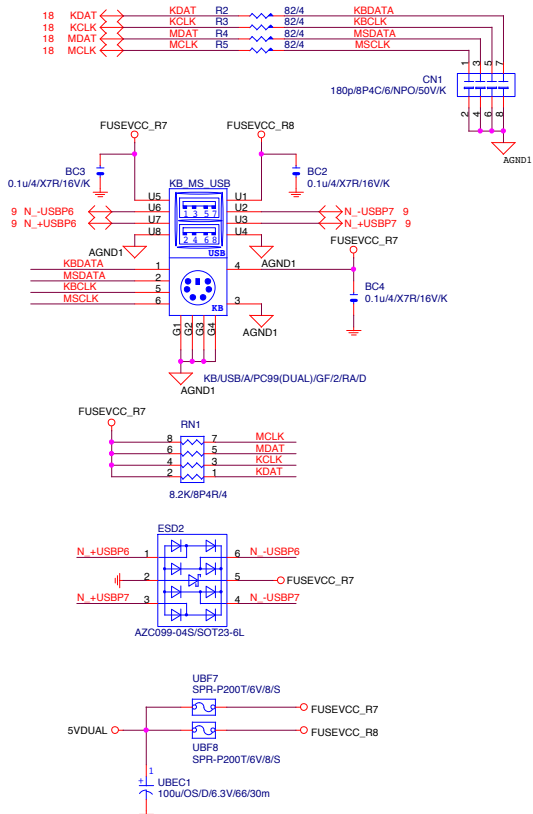


VOLTAGE-- H/W MONITOR

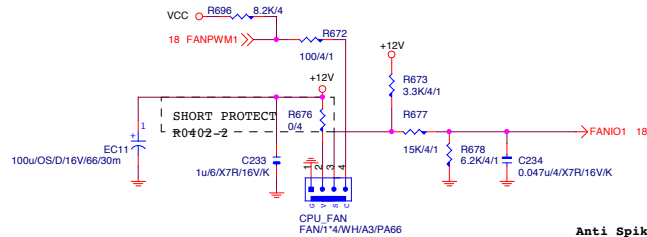


The division voltage of VIN2 & VIN3 must be around 2.9V

## KB/USB

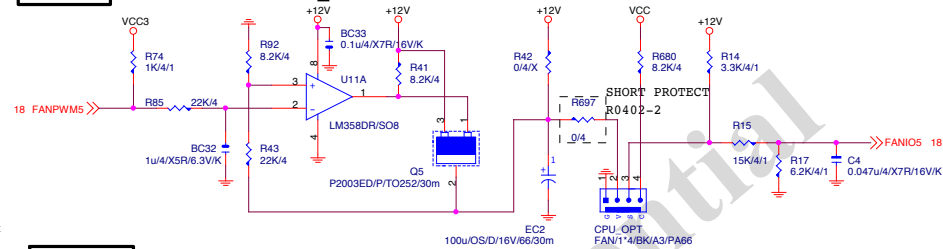


## CPU FAN



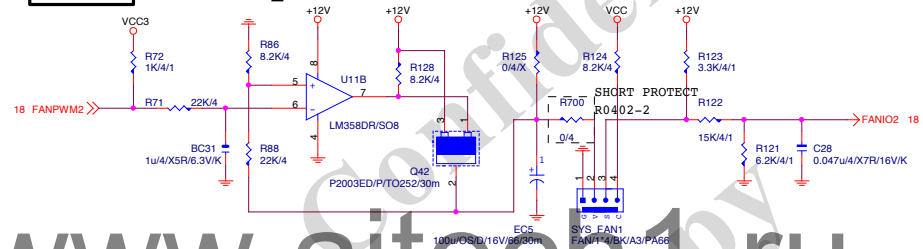
## CPU\_ OPT

### Linear CPU OPT



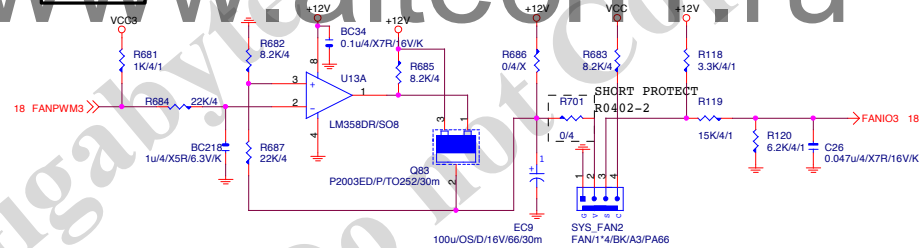
## SYS FAN\_1

Linear SYS FAN



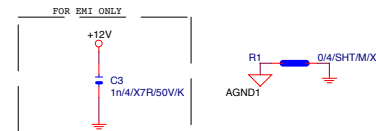
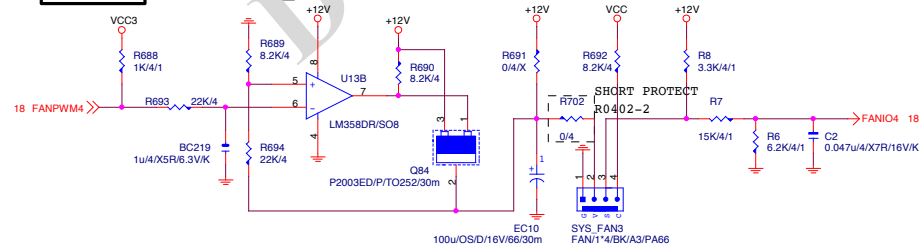
## SYS\_FAN\_2

Linear SYS\_FAN



## SYS FAN\_3

Linear SYS FAN

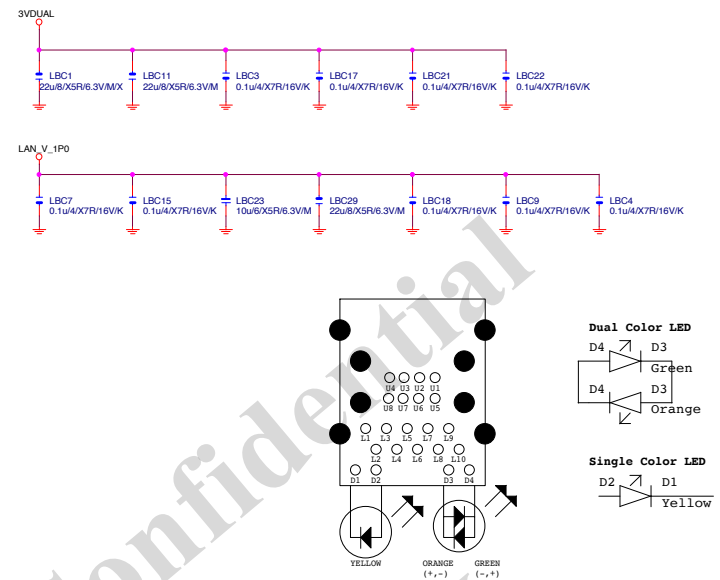
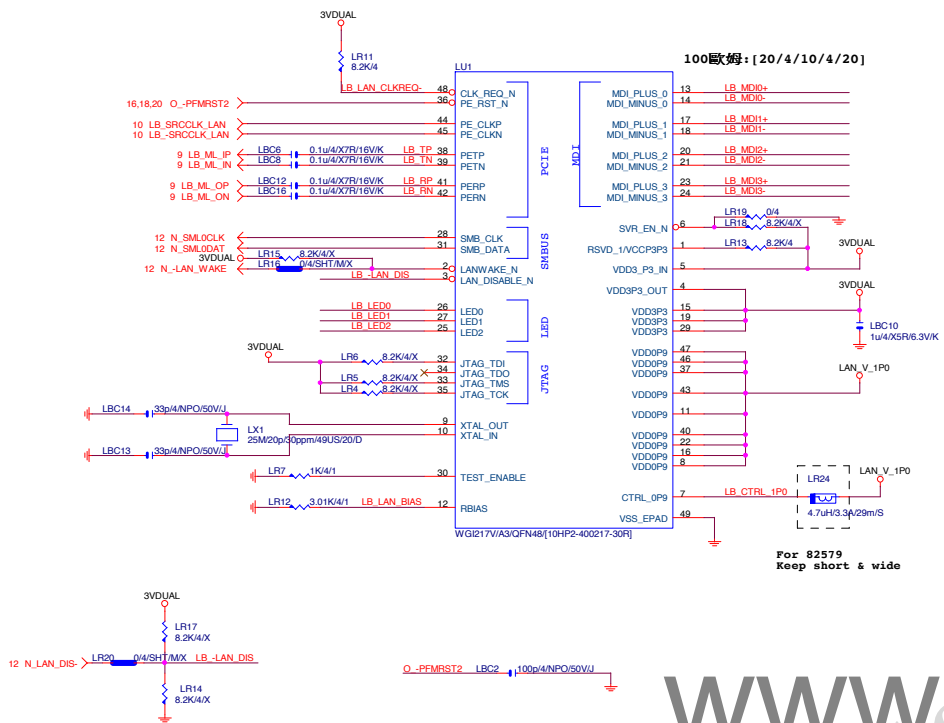


## Gigabyte Technology

Title				HWM,KB/MS, FAN CTRL			
Size		Document Number					Rev
Custom		GA-H87-D3H					1.1
Date: Tuesday, August 06, 2013				Sheet 30 of 34			

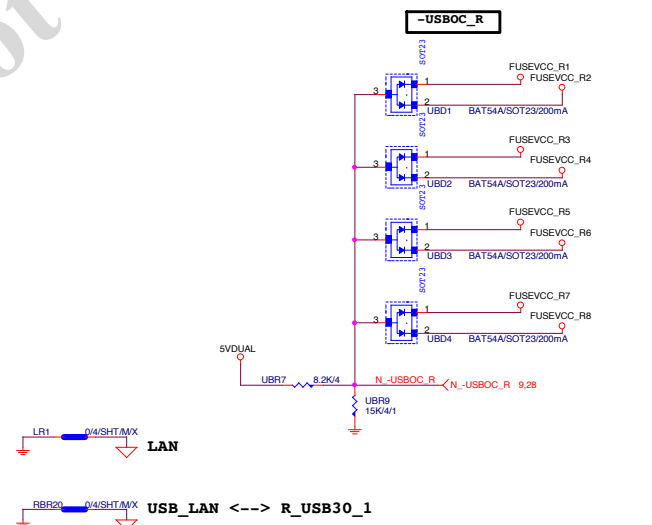
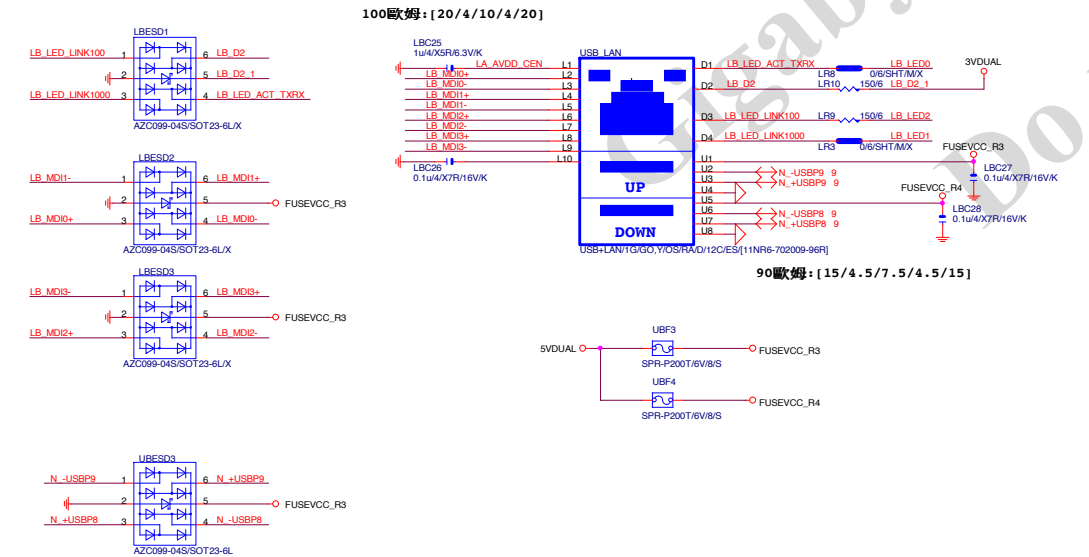


# LAN:INTEL I217



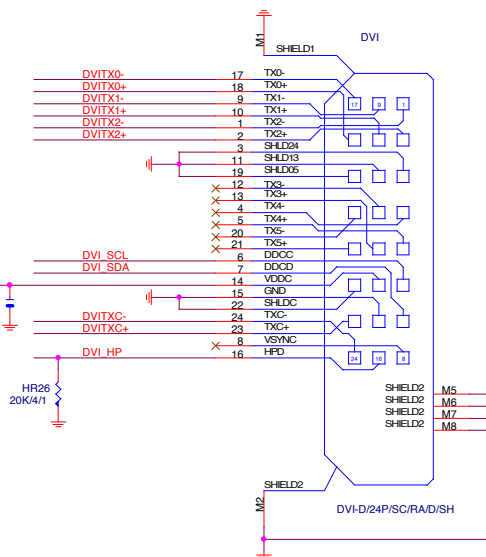
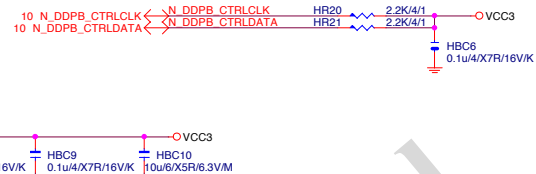
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## USB30 LAN CONNECTOR





**DVI: 15/4/4/4/15**  
**Impedance=85 +- 17.5%**



<b><i>Gigabyte Technology</i></b>			
<b>TI TSB43AB23 1394</b>			
Size Custom	Document Number	<b>GA-H87-D3H</b>	<b>1.1</b>
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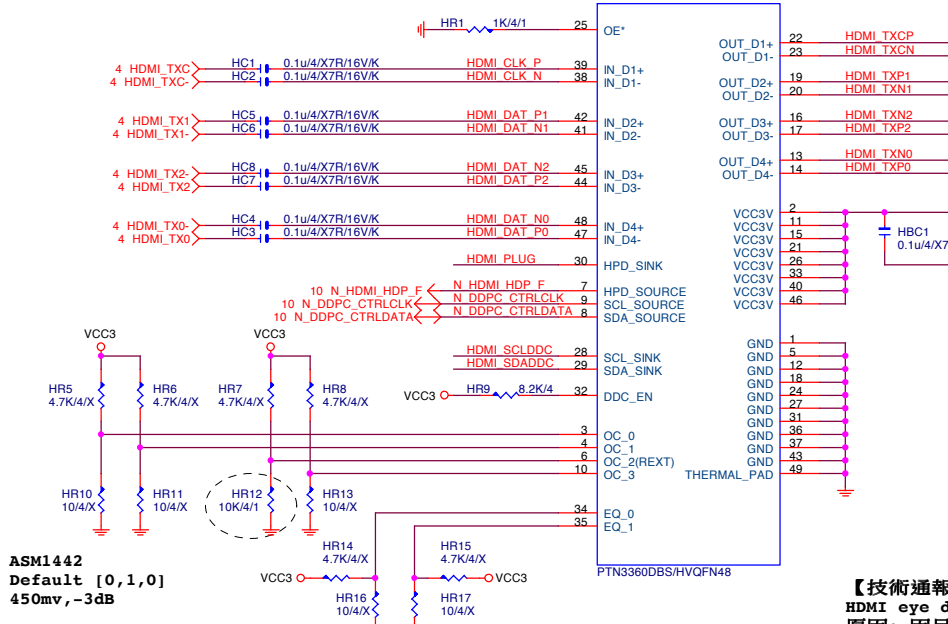


# HDMI LEVEL SHIFT

HDMI:15/4/4/15

Impedance=85 +- 17.5%

HU1



ASM1442  
Default [0,1,0]  
450mv, -3dB

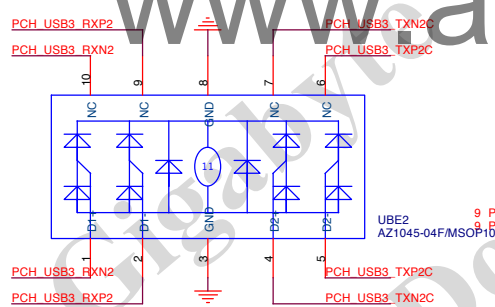
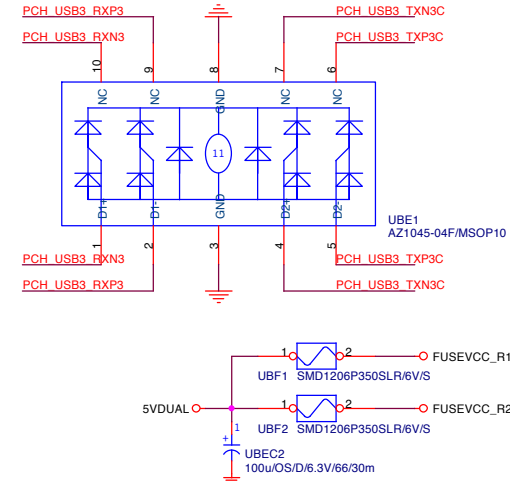
ASM1442 Default [0,0] 3dB  
[0,1] 6dB

## 【技術通報R&D技術通報150】

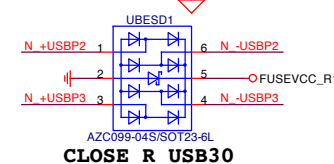
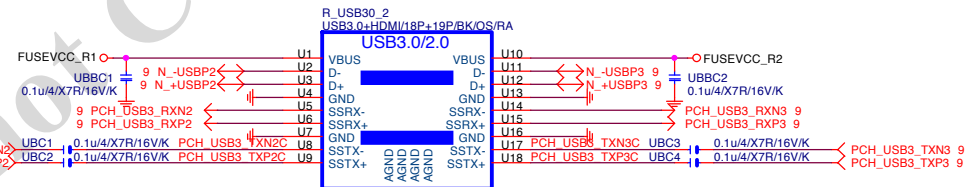
HDMI eye diagram1.4版(deep color)會fail

原因: 因目前的HDMI訊號過長,造成RISING TIME過慢,而會壓到eye diagram

改善: ASMEDIA ASM1442 : 3.16K(PIN6 PULL DOWN電阻) 10ohm(PIN4 PULL DOWN電阻)



## R\_USB30



GIGABYTE™			
Title			
HDMI & USB			
Size	Document Number	Rev	
Custom	GA-H87-D3H	1.1	
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